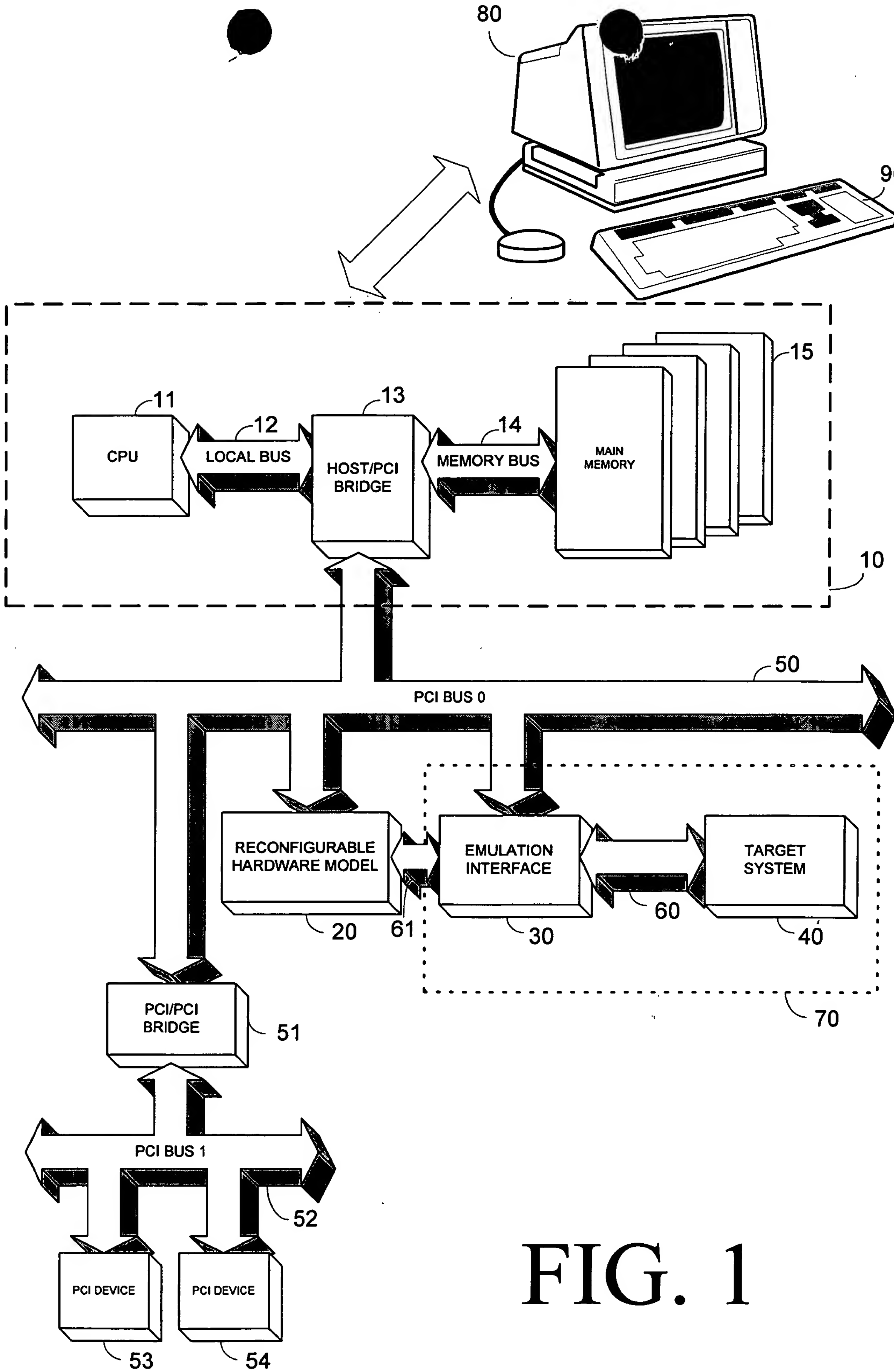

80
90
15
11
12
13
14
CPU
LOCAL BUS
HOST/PCI
BRIDGE
MEMORY BUS
MAIN
MEMORY
10
50
PCI BUS 0
RECONFIGURABLE
HARDWARE MODEL
EMULATION
INTERFACE
TARGET
SYSTEM
20
61
30
60
40
70
PCI/PCI
BRIDGE
51
PCI BUS 1
52
PCI DEVICE
PCI DEVICE
53
54

FIG. 1

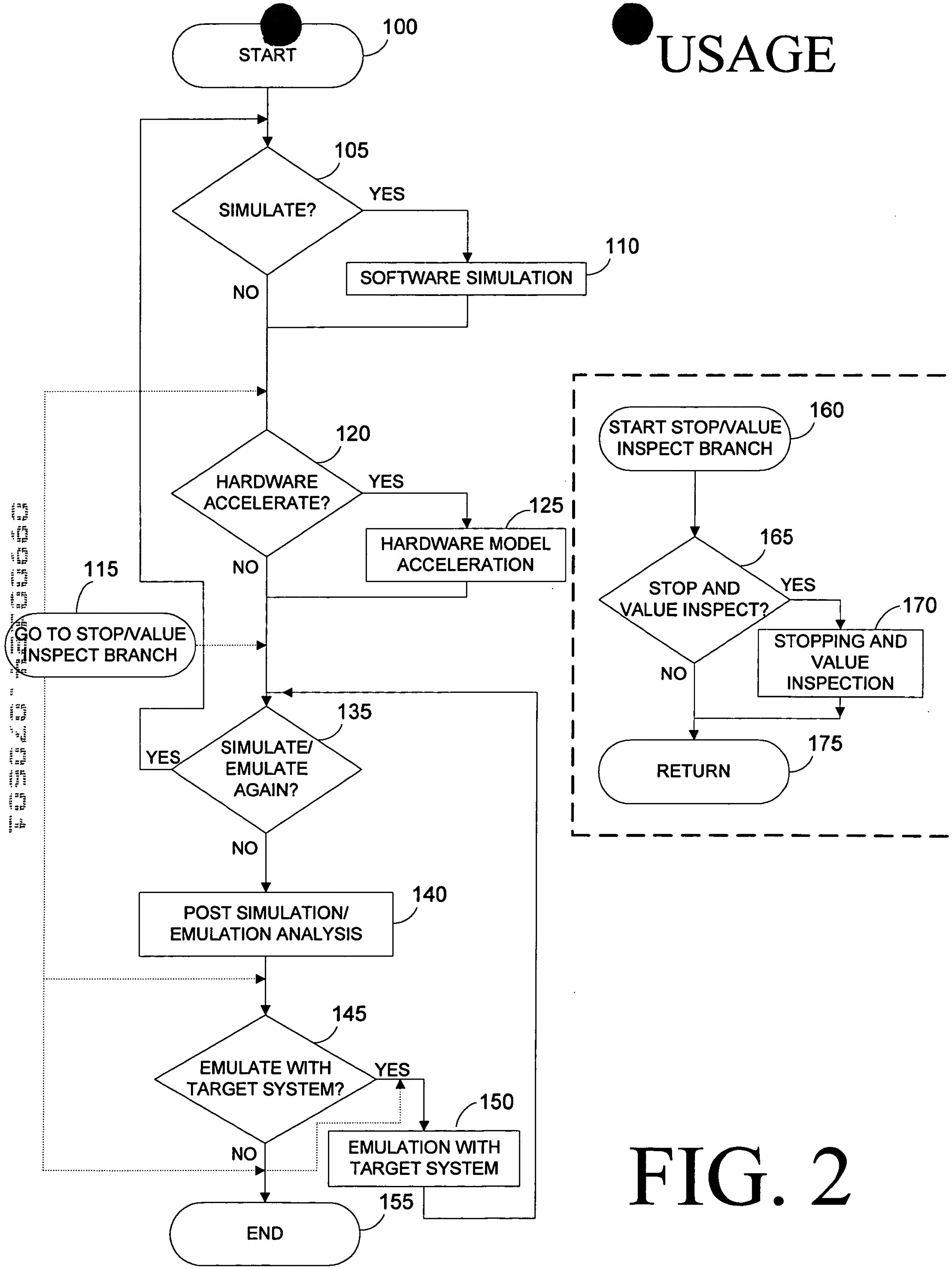

USAGE
START
100
SIMULATE?
105
YES
SOFTWARE SIMULATION
110
NO
HARDWARE ACCELERATE?
120
YES
HARDWARE MODEL ACCELERATION
125
NO
115
GO TO STOP/VALUE INSPECT BRANCH
SIMULATE/ EMULATE AGAIN?
135
YES
NO
POST SIMULATION/ EMULATION ANALYSIS
140
EMULATE WITH TARGET SYSTEM?
145
YES
EMULATION WITH TARGET SYSTEM
150
NO
END
155
START STOP/VALUE INSPECT BRANCH
160
STOP AND VALUE INSPECT?
165
YES
STOPPING AND VALUE INSPECTION
170
NO
RETURN
175

FIG. 2

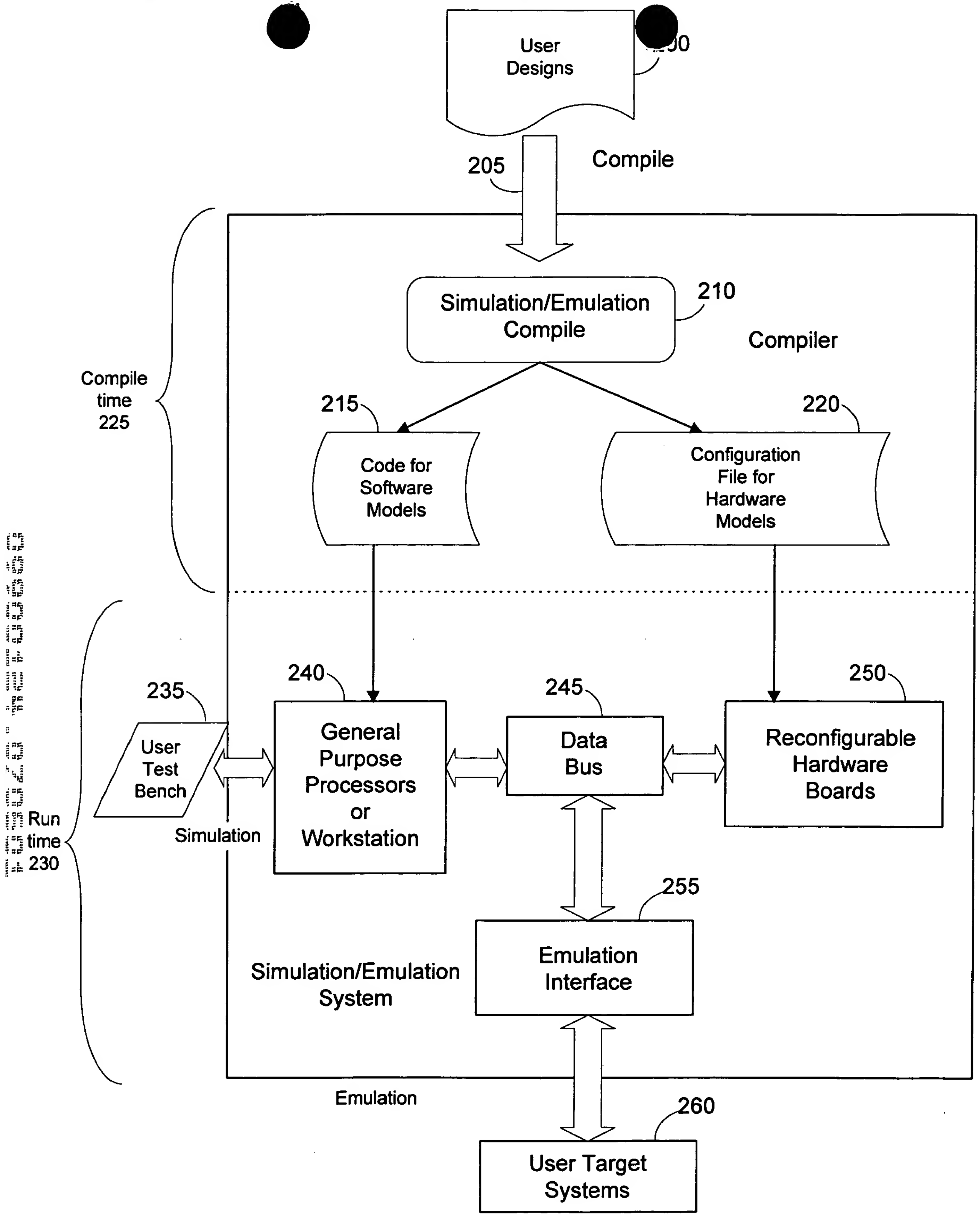

User Designs
200
205
Compile
Simulation/Emulation Compile
210
Compiler
Compile time 225
215
Code for Software Models
220
Configuration File for Hardware Models
235
User Test Bench
240
General Purpose Processors or Workstation
245
Data Bus
250
Reconfigurable Hardware Boards
Run time 230
Simulation
255
Emulation Interface
Simulation/Emulation System
Emulation
260
User Target Systems

FIG. 3

COMPILATION

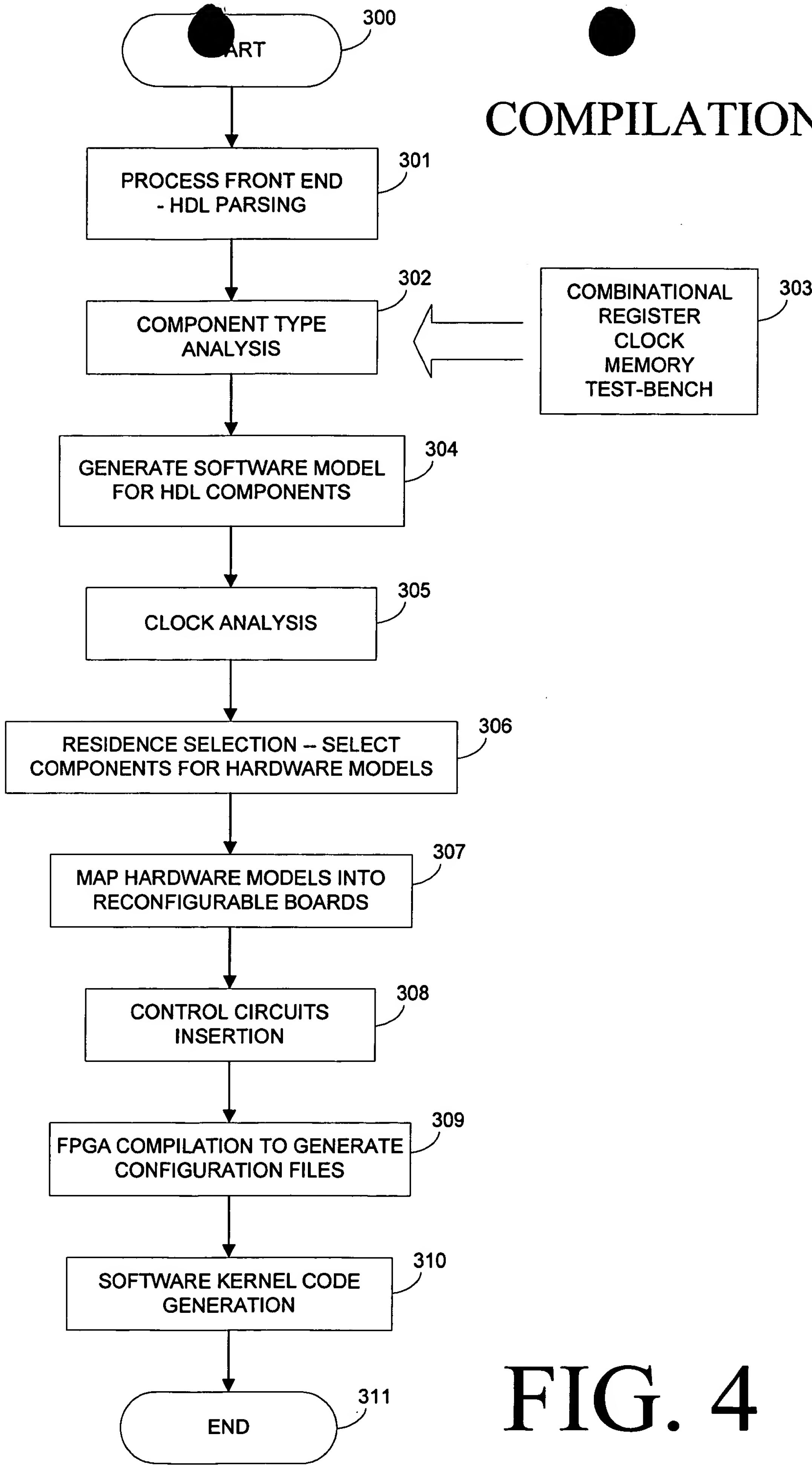


FIG. 4

SOFTWARE KERNEL

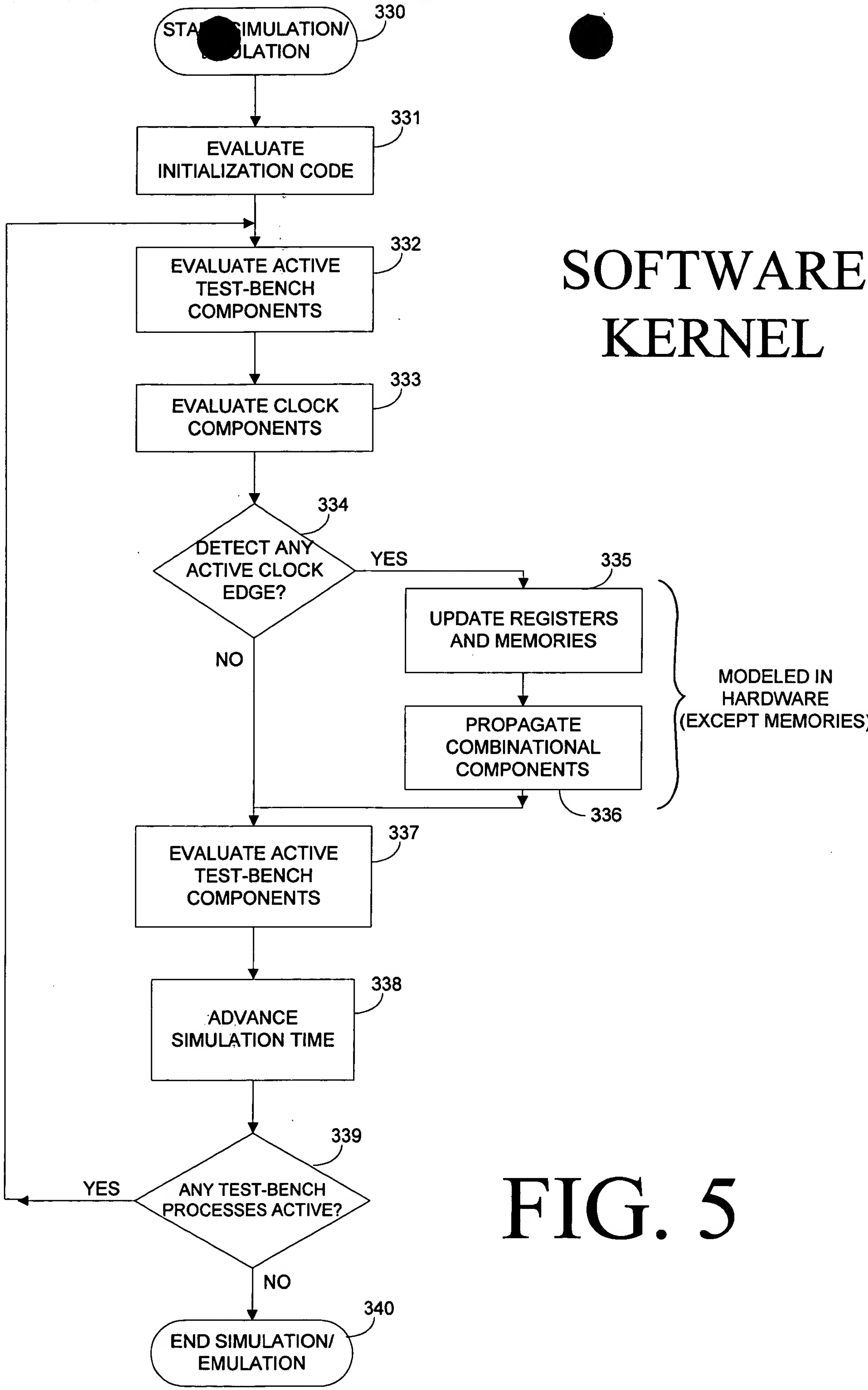


FIG. 5

MAPPING HARDWARE MODELS TO RECONFIGURABLE BOARDS

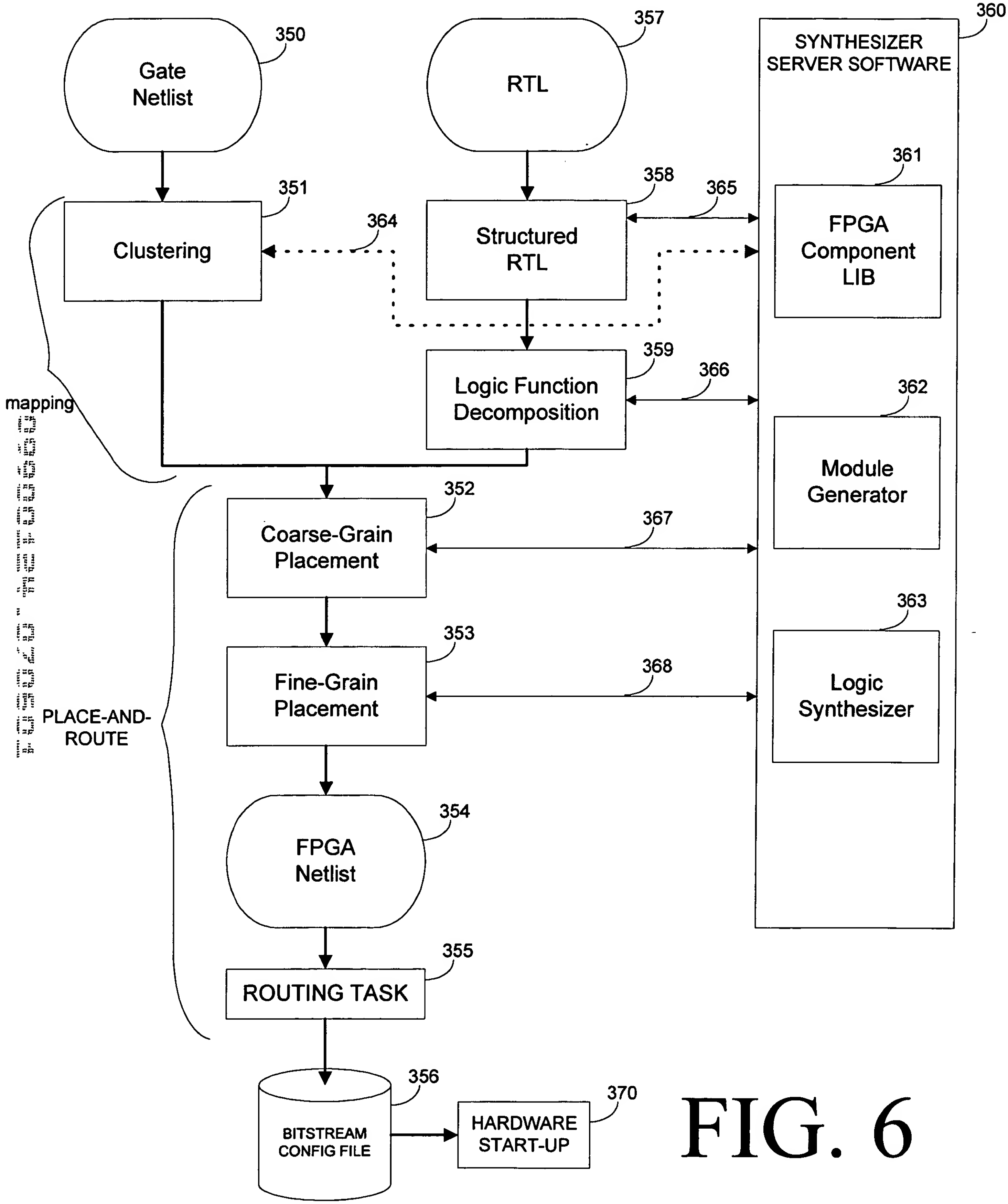


FIG. 6

	F11	F12	F13	F14	F21	F22	F23	F24	F31	F32	F33	F34	F41	F42	F43	F44
F11	1	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0
F12	1	1	1	1	0	1	0	0	0	1	0	0	0	1	0	0
F13	1	1	1	1	0	0	1	0	0	0	1	0	0	0	1	0
F14	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1
F21	0	0	0	0	1	1	1	1	1	0	0	0	1	0	0	0
F22	1	1	0	0	1	1	1	1	0	1	0	0	0	1	0	0
F23	0	0	1	0	1	1	1	1	0	0	1	0	0	0	1	0
F24	0	0	0	1	1	1	1	1	0	0	0	1	0	0	0	1
F31	0	0	0	0	1	0	0	0	1	1	1	1	1	0	0	0
F32	1	1	0	0	0	1	0	0	1	1	1	1	0	1	0	0
F33	0	0	1	0	0	0	1	0	1	1	1	1	0	0	1	0
F34	0	0	0	1	0	0	0	1	1	1	1	1	0	0	0	1
F41	0	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1
F42	1	1	0	0	0	1	0	0	0	1	0	0	1	1	1	1
F43	0	0	1	0	0	0	1	0	0	0	1	0	1	1	1	1
F44	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	1

FIG. 7

FPGA INTERCONNECTION

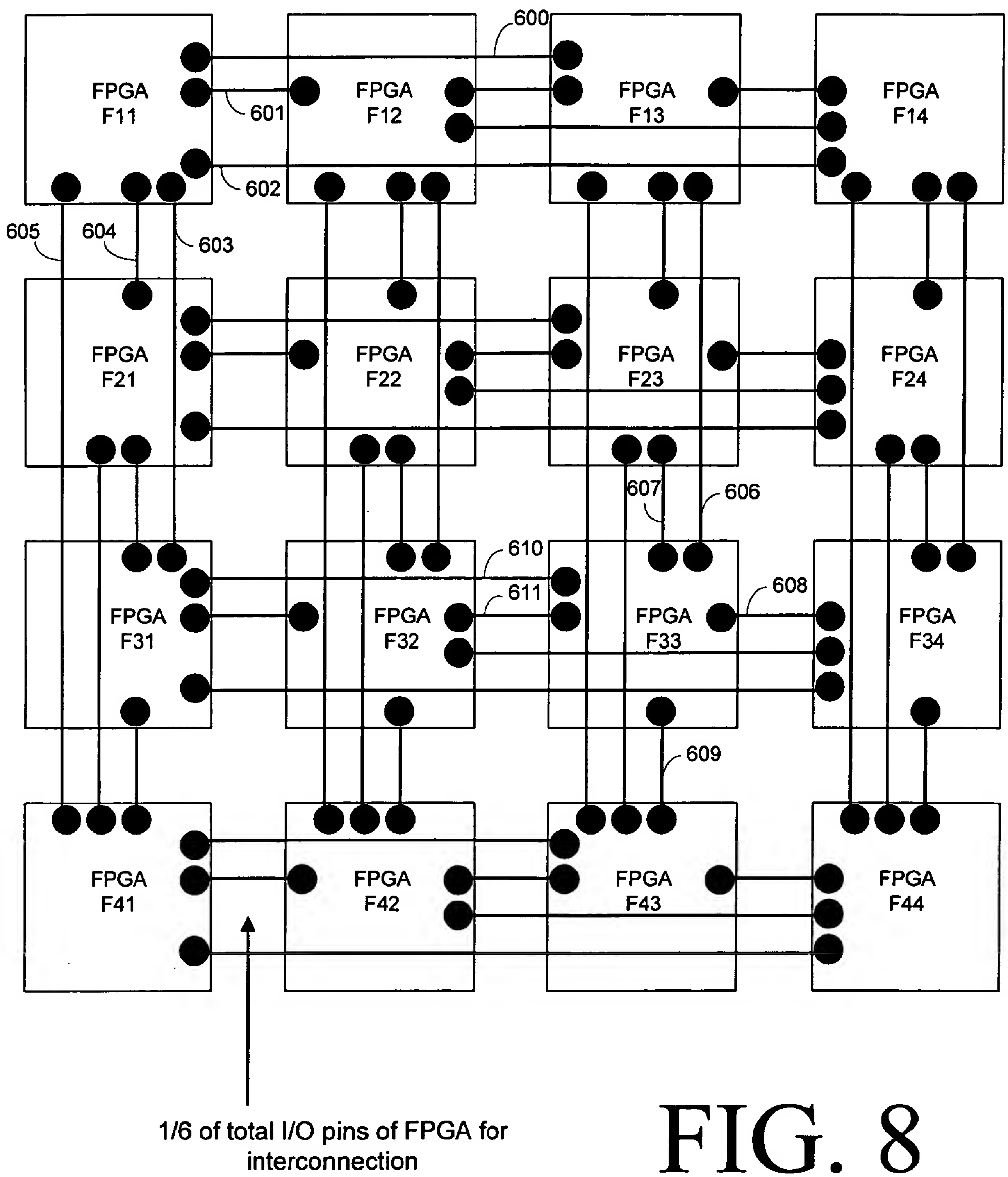


FIG. 8

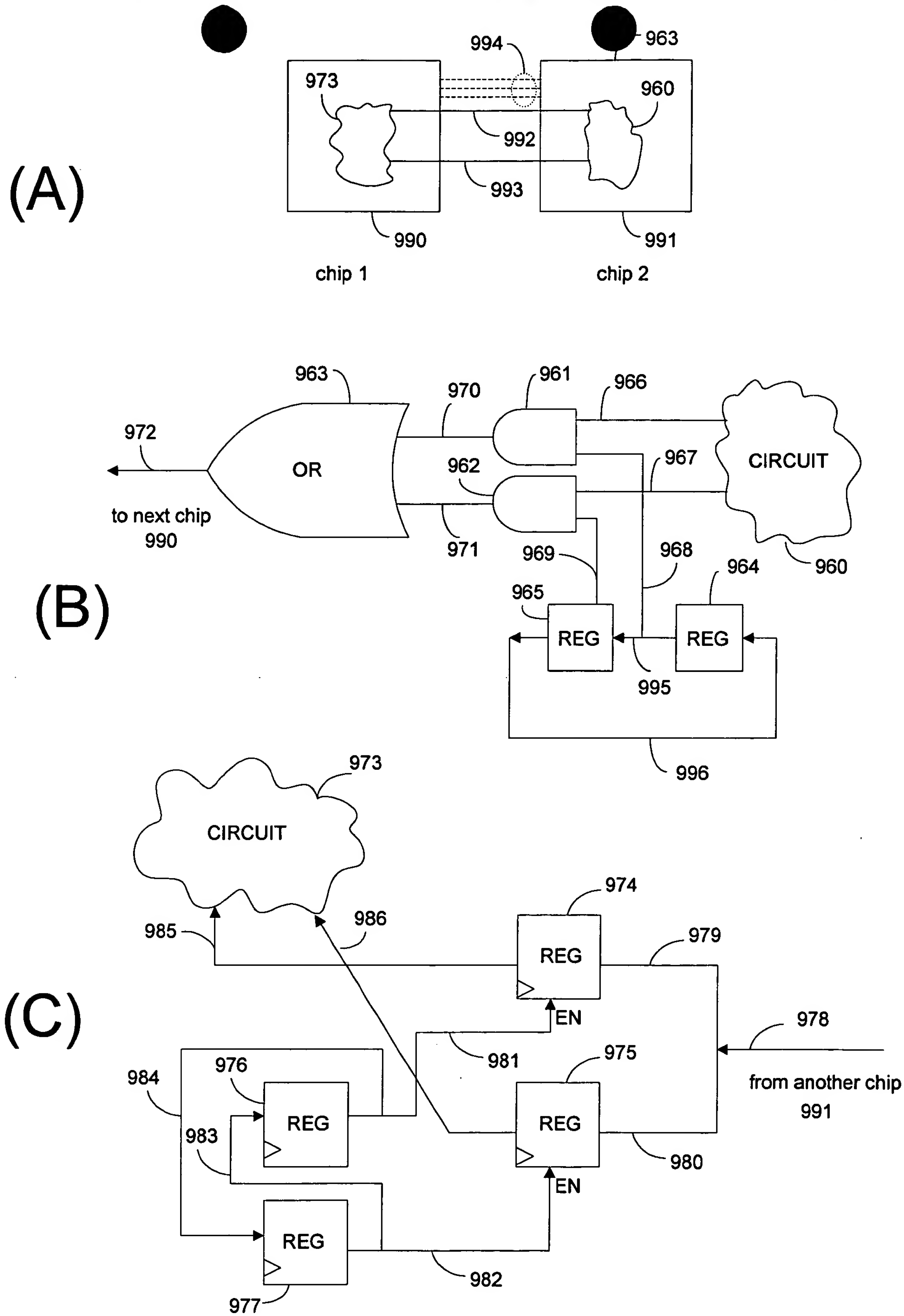

(A)
994
963
973
960
992
993
990
991
chip 1
chip 2
(B)
963
970
961
966
972
OR
962
967
CIRCUIT
to next chip
990
971
969
968
964
960
965
REG
REG
995
996
(C)
973
CIRCUIT
974
985
986
REG
979
EN
978
981
975
984
976
REG
REG
from another chip
991
983
980
EN
REG
982
977

FIG. 9

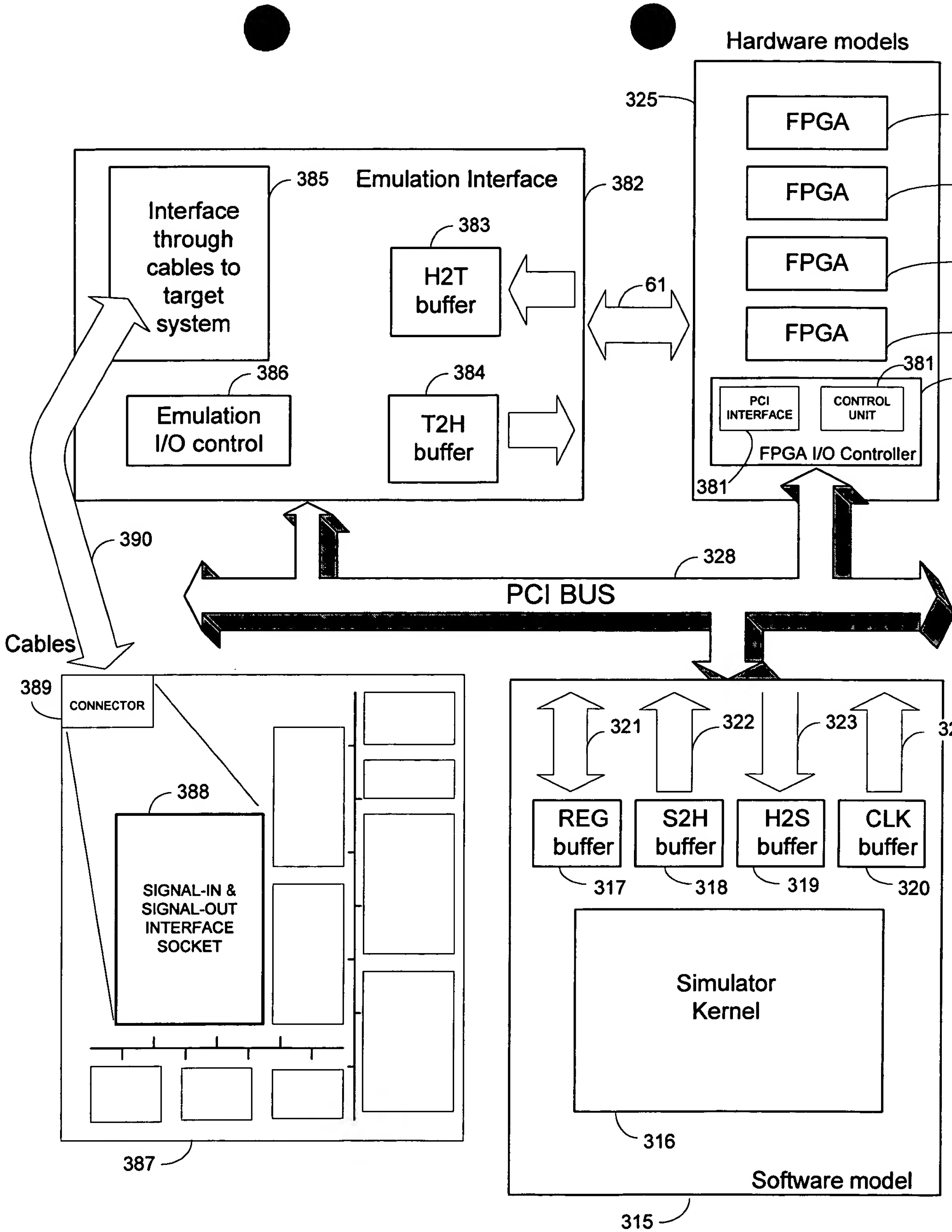

Hardware models
325
FPGA
326a
FPGA
326b
FPGA
326c
FPGA
326d
381
327
PCI INTERFACE
CONTROL UNIT
FPGA I/O Controller
381
Emulation Interface
382
385
Interface through cables to target system
383
H2T buffer
61
386
Emulation I/O control
384
T2H buffer
390
328
PCI BUS
Cables
389
CONNECTOR
388
SIGNAL-IN & SIGNAL-OUT INTERFACE SOCKET
387
321
322
323
324
REG buffer
S2H buffer
H2S buffer
CLK buffer
317
318
319
320
Simulator Kernel
316
Software model
315

FIG. 10

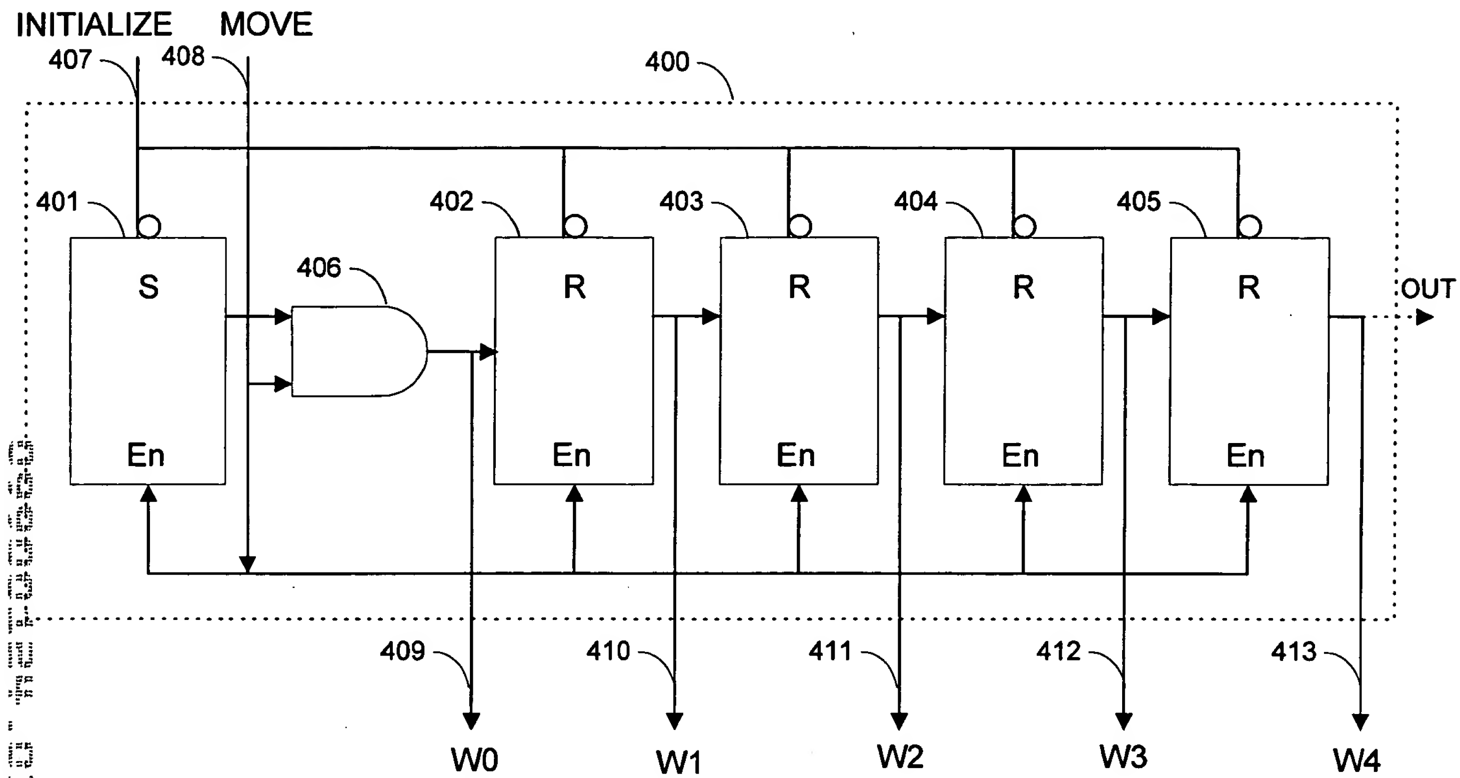

INITIALIZE
MOVE
407
408
400
401
402
403
404
405
406
S
R
R
R
R
En
En
En
En
En
OUT
409
410
411
412
413
W0
W1
W2
W3
W4

FIG. 11

ADDRESS POINTER INITIALIZATION

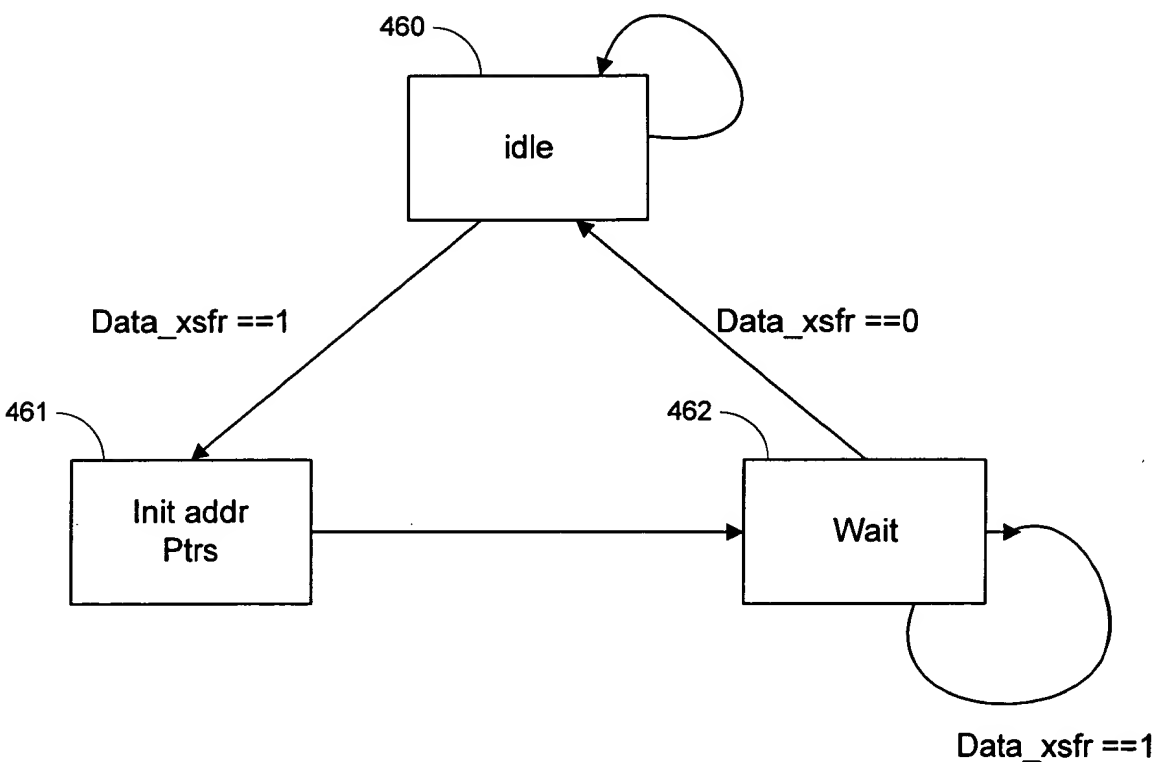
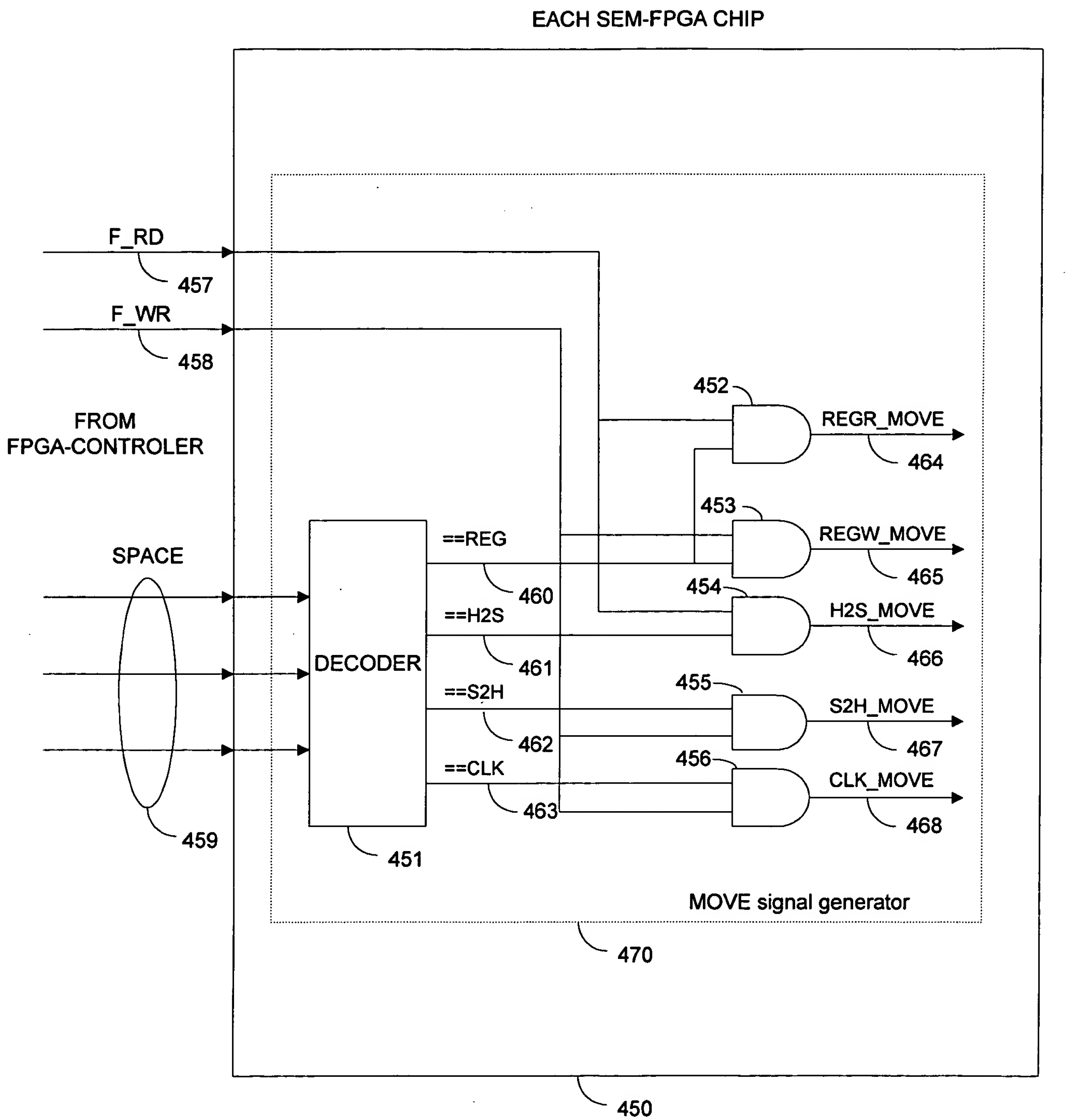


FIG. 12



EACH SEM-FPGA CHIP
F_RD
457
F_WR
458
FROM
FPGA-CONTROLER
SPACE
459
DECODER
451
==REG
460
==H2S
461
==S2H
462
==CLK
463
452
453
454
455
456
REGR_MOVE
464
REGW_MOVE
465
H2S_MOVE
466
S2H_MOVE
467
CLK_MOVE
468
MOVE signal generator
470
450

FIG. 13

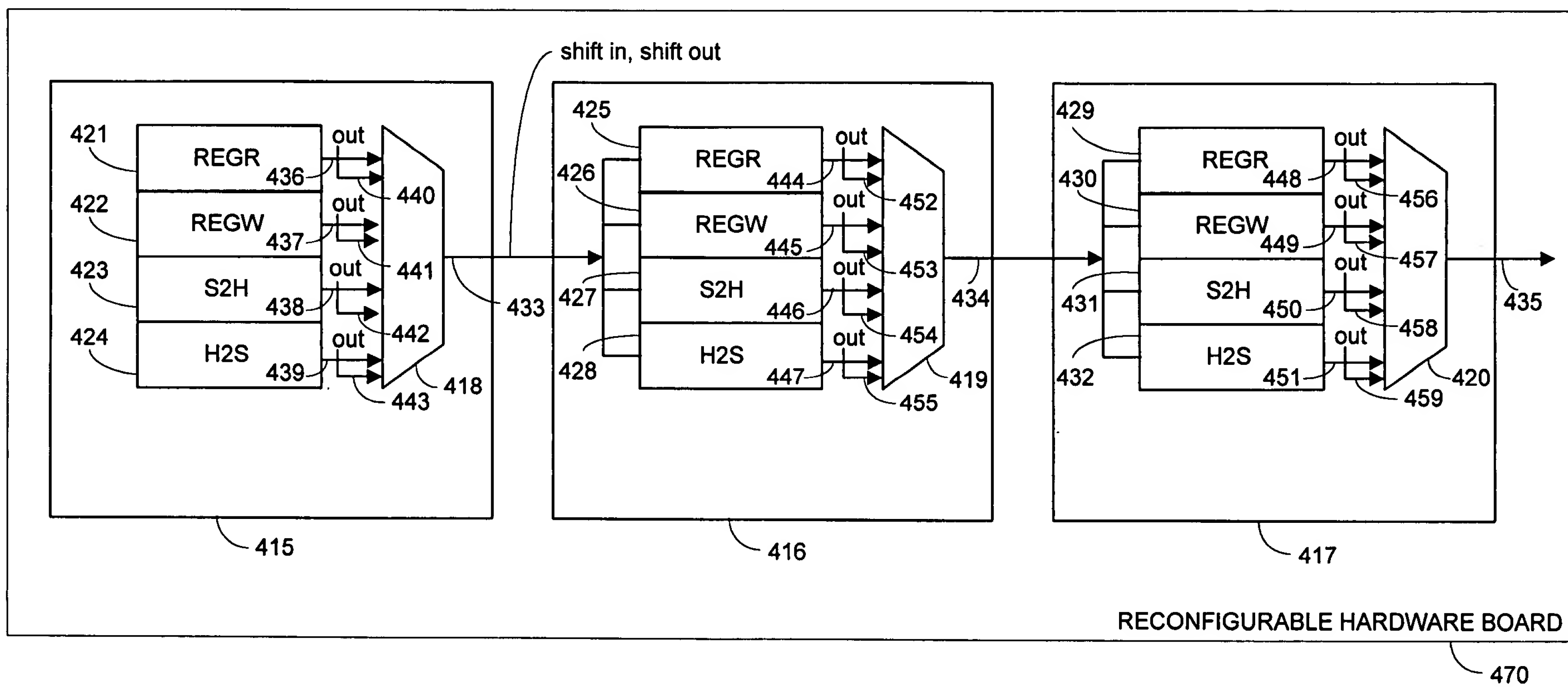

shift in, shift out
REGR
REGW
S2H
H2S
out
RECONFIGURABLE HARDWARE BOARD
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
470

FIG. 14

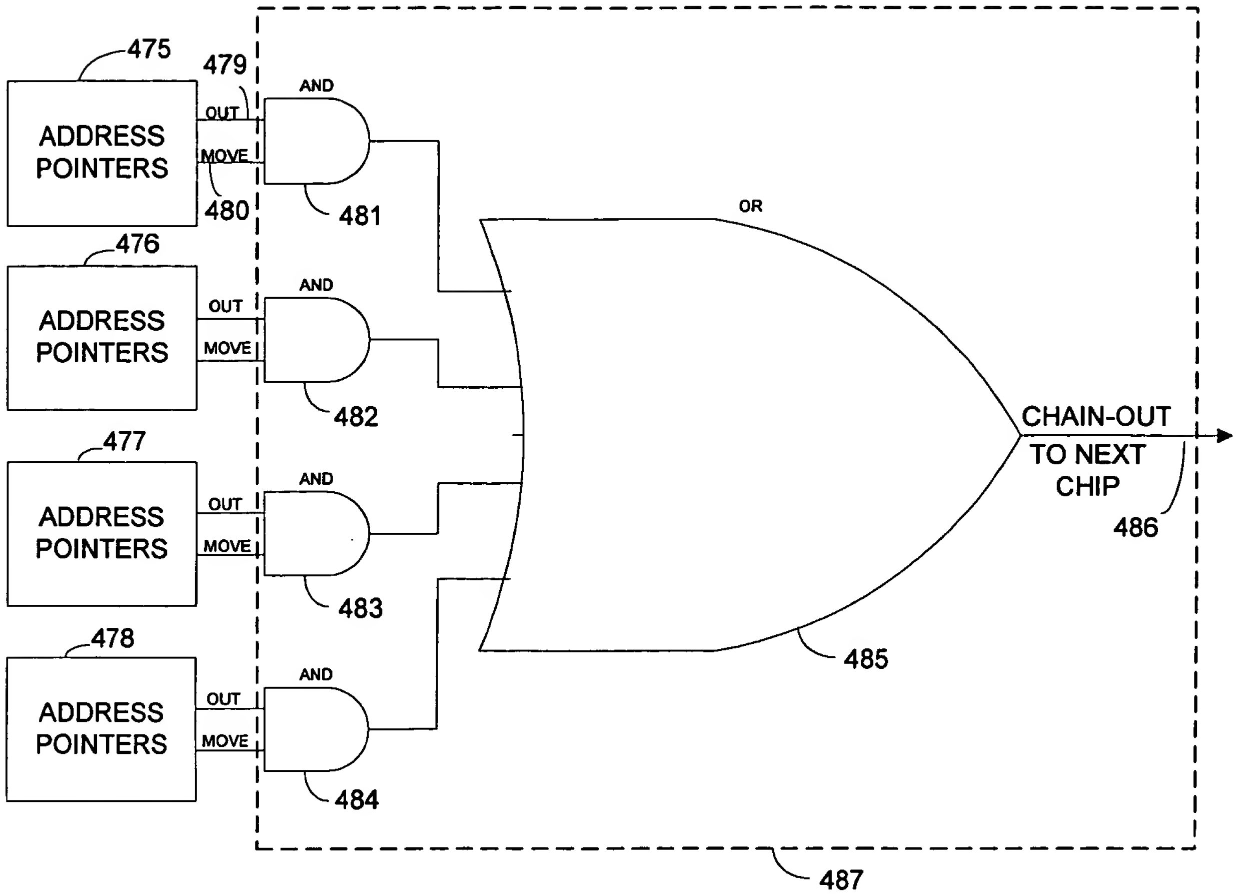

475
476
477
478
ADDRESS POINTERS
ADDRESS POINTERS
ADDRESS POINTERS
ADDRESS POINTERS
479
480
OUT
MOVE
OUT
MOVE
OUT
MOVE
OUT
MOVE
AND
AND
AND
AND
481
482
483
484
OR
485
CHAIN-OUT TO NEXT CHIP
486
487

FIG. 15

GATED DATA/CLOCK ANALYSIS

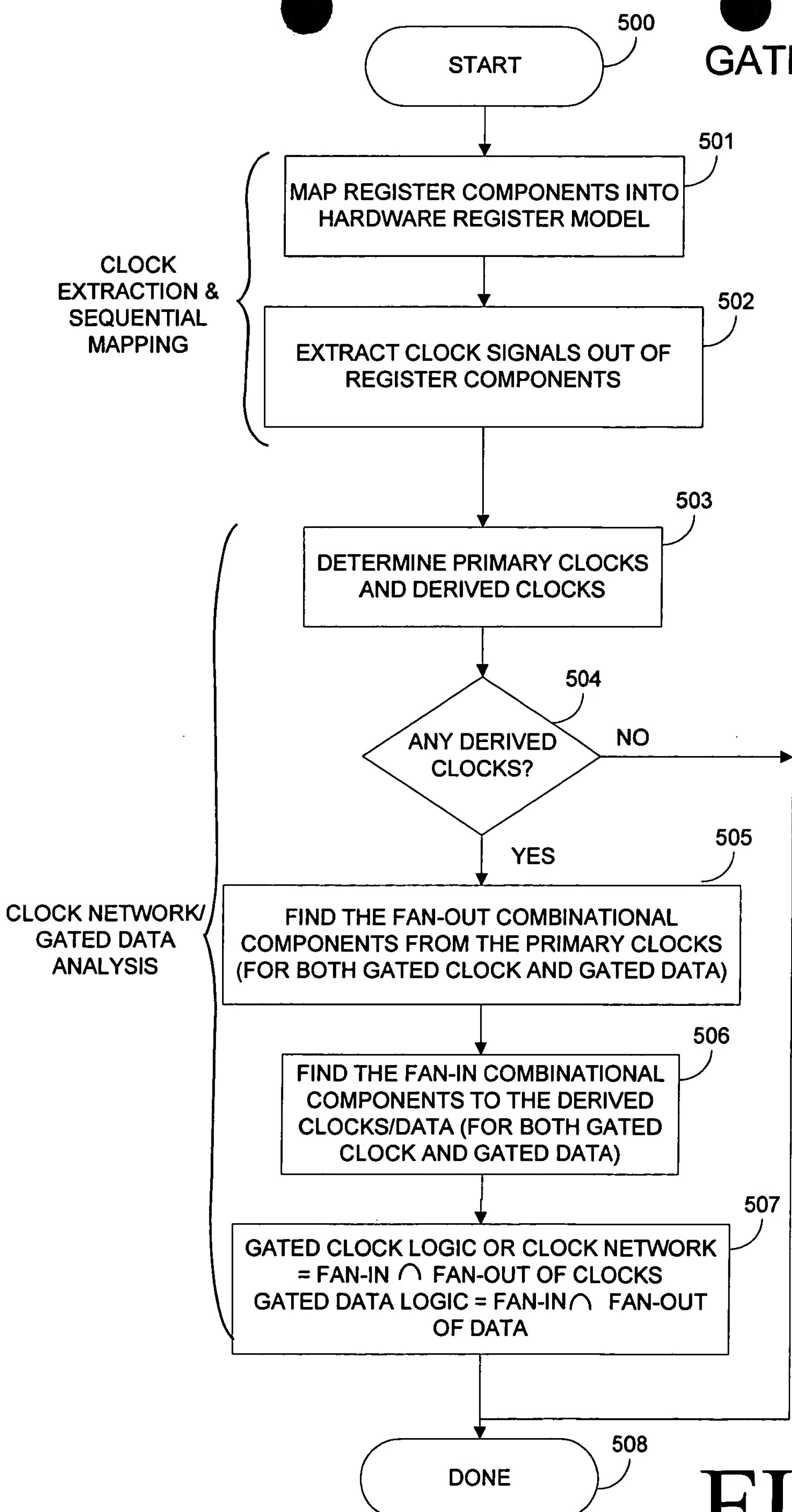


FIG. 16

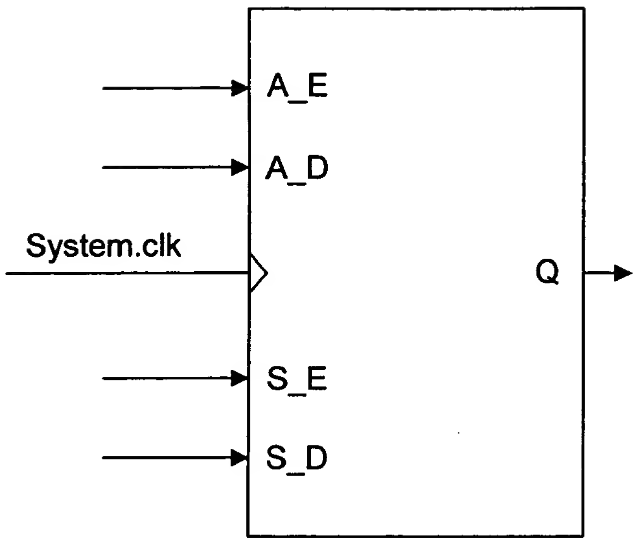


FIG. 17

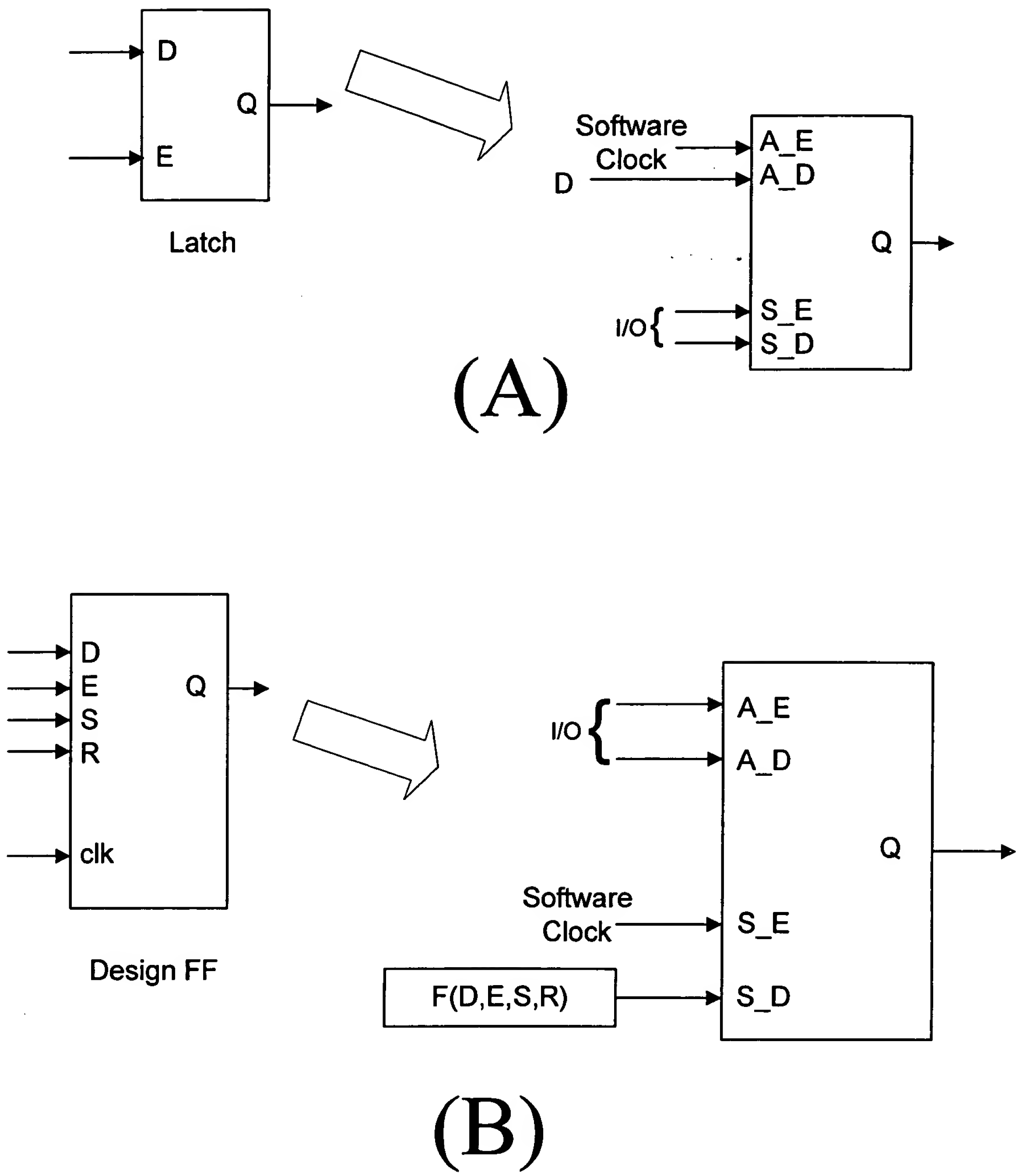

D
E
Q
Latch
Software
Clock
D
A_E
A_D
Q
I/O
S_E
S_D
(A)
D
E
S
R
clk
Q
Design FF
I/O
A_E
A_D
Q
Software
Clock
S_E
F(D,E,S,R)
S_D
(B)

FIG. 18

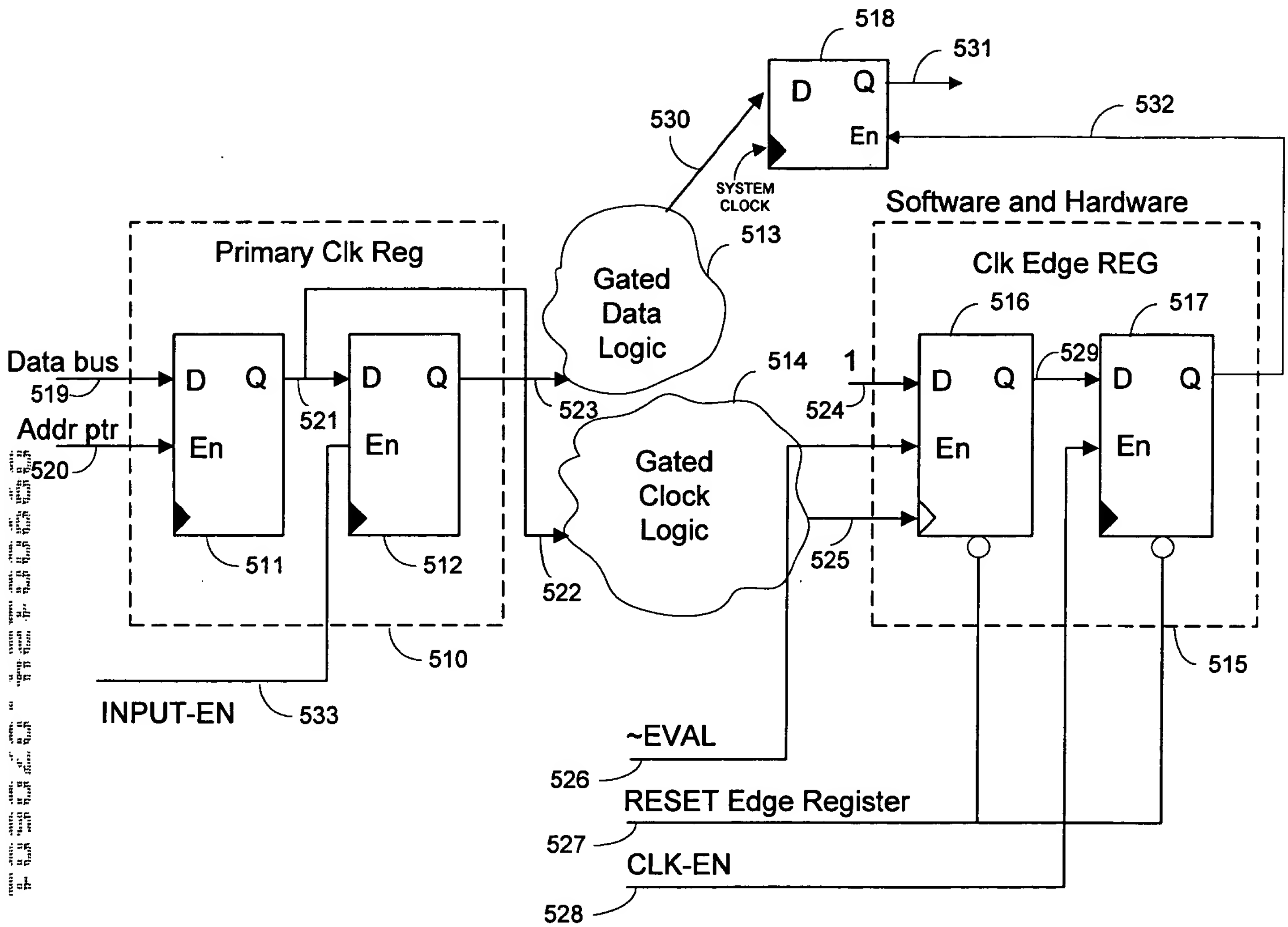

518
531
D
Q
En
530
SYSTEM CLOCK
532
Software and Hardware
513
Primary Clk Reg
Gated Data Logic
Clk Edge REG
516
517
Data bus
519
D
Q
En
521
D
Q
En
523
514
1
524
529
D
Q
En
D
Q
En
Addr ptr
520
Gated Clock Logic
511
512
522
525
510
515
INPUT-EN
533
~EVAL
526
RESET Edge Register
527
CLK-EN
528

FIG. 19

DURING EVALUATION

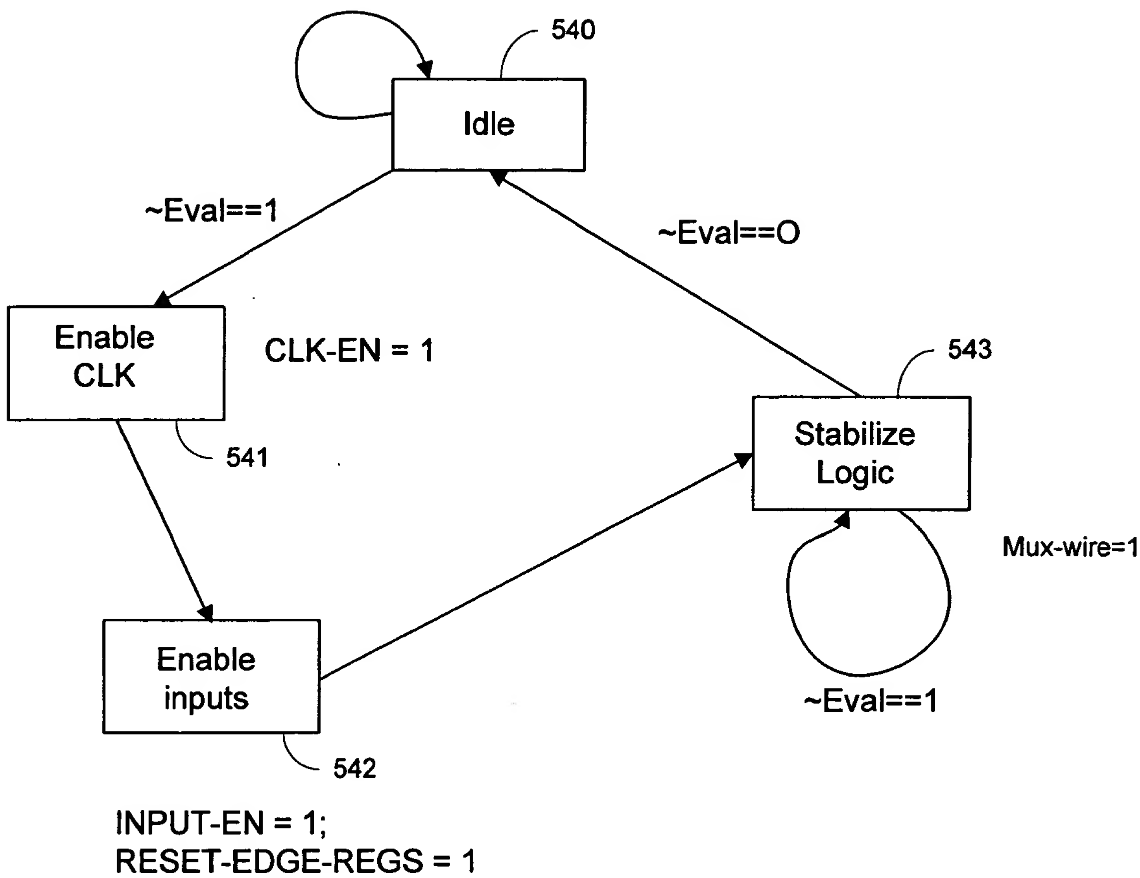


FIG. 20

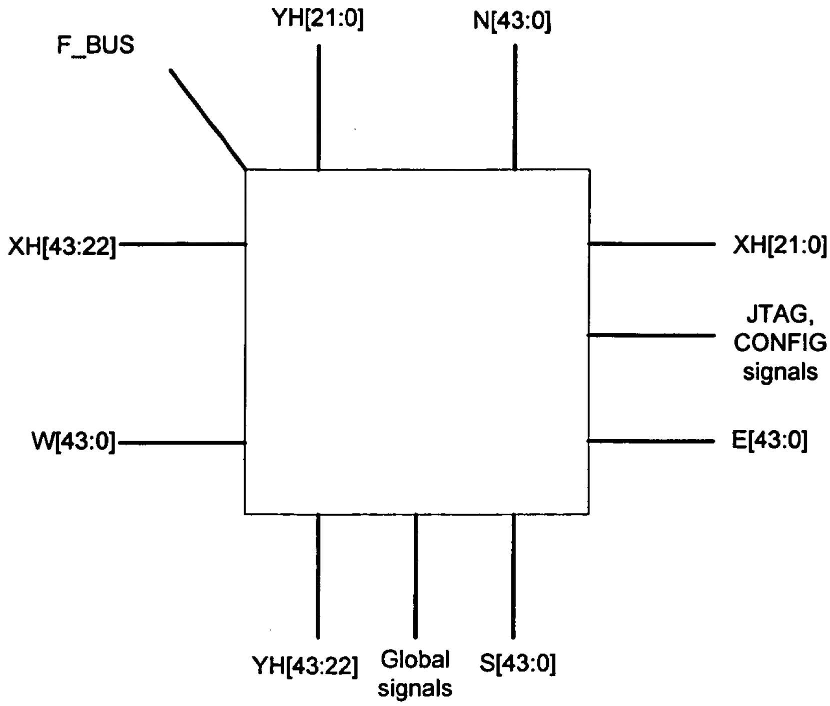

F_BUS
YH[21:0]
N[43:0]
XH[43:22]
XH[21:0]
JTAG, CONFIG signals
W[43:0]
E[43:0]
YH[43:22]
Global signals
S[43:0]

FIG. 21

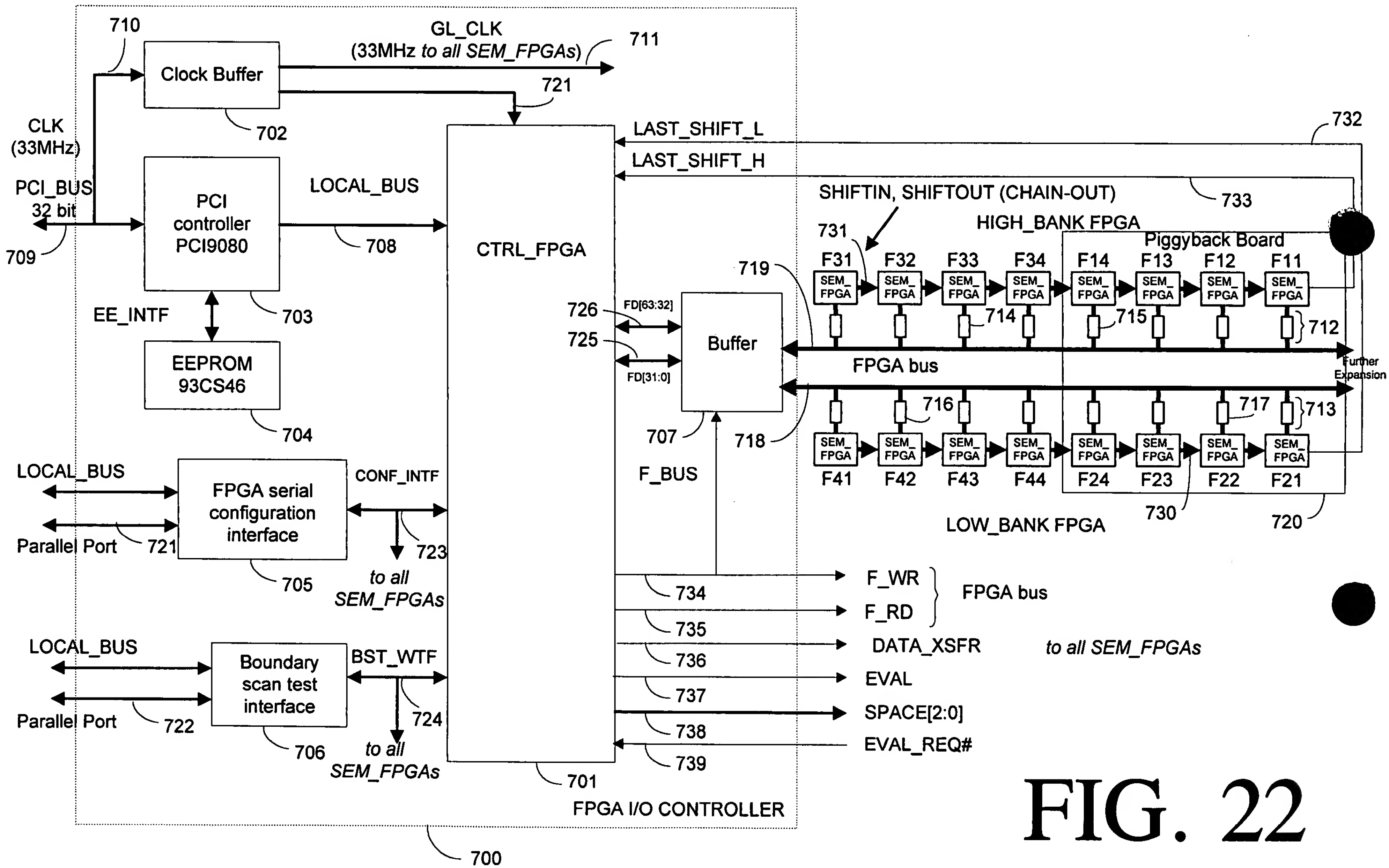

GL_CLK
(33MHz to all SEM_FPGAs)
711
710
Clock Buffer
721
702
CLK
(33MHz)
PCI_BUS
32 bit
709
PCI
controller
PCI9080
703
LOCAL_BUS
708
EE_INTF
EEPROM
93CS46
704
CTRL_FPGA
LAST_SHIFT_L
LAST_SHIFT_H
732
733
SHIFTIN, SHIFTOUT (CHAIN-OUT)
HIGH_BANK FPGA
Piggyback Board
731
F31
F32
F33
F34
F14
F13
F12
F11
SEM_
FPGA
719
726
725
FD[63:32]
FD[31:0]
Buffer
714
715
712
FPGA bus
Further
Expansion
716
717
713
707
718
F41
F42
F43
F44
F24
F23
F22
F21
F_BUS
LOW_BANK FPGA
730
720
LOCAL_BUS
FPGA serial
configuration
interface
CONF_INTF
Parallel Port
721
723
705
to all
SEM_FPGAs
F_WR
F_RD
FPGA bus
734
735
DATA_XSFR
to all SEM_FPGAs
736
EVAL
737
SPACE[2:0]
738
EVAL_REQ#
739
LOCAL_BUS
Boundary
scan test
interface
BST_WTF
Parallel Port
722
724
706
to all
SEM_FPGAs
701
FPGA I/O CONTROLLER
700

FIG. 22

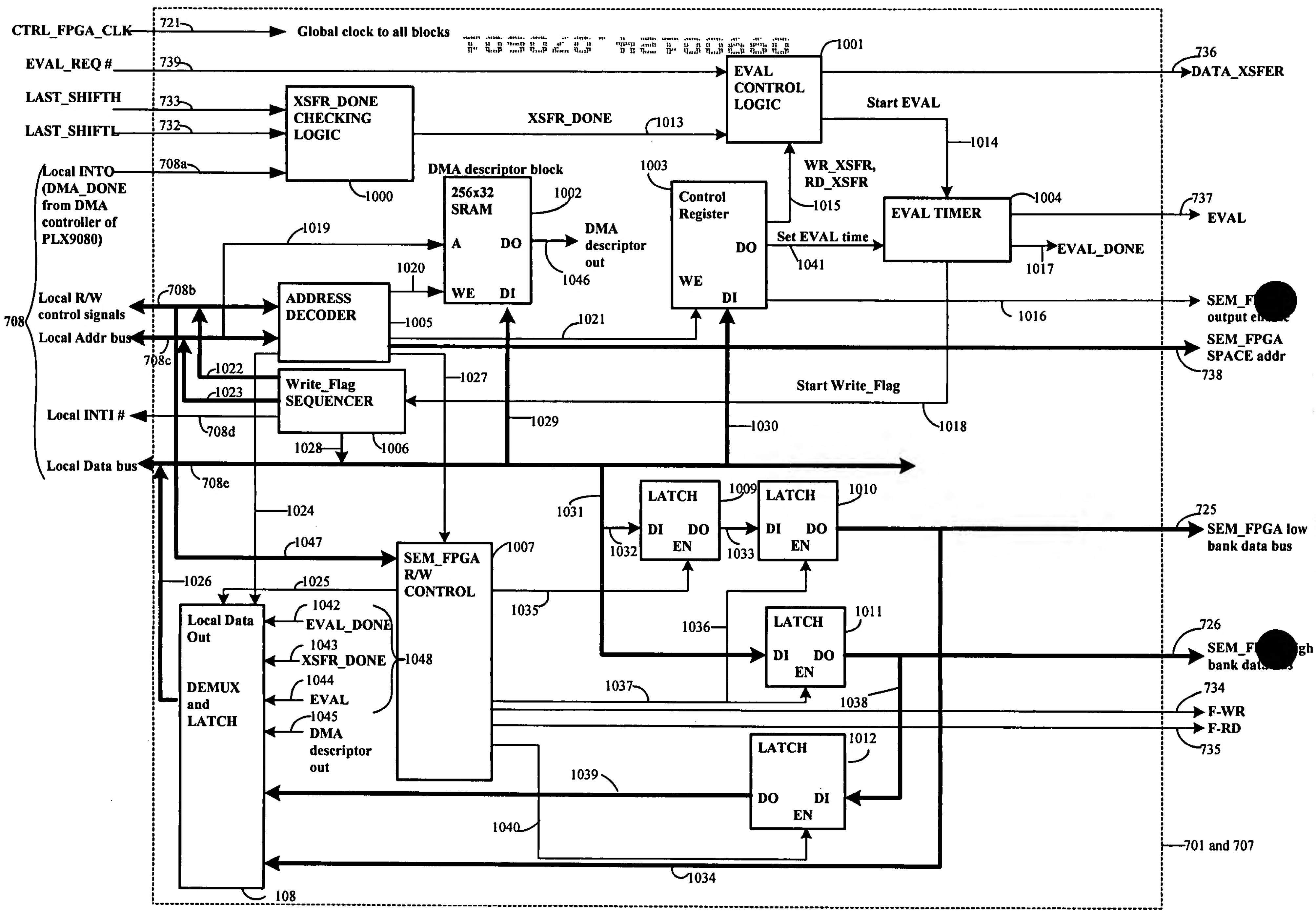

CTRL_FPGA_CLK
721
Global clock to all blocks
EVAL_REQ #
739
LAST_SHIFTH
733
LAST_SHIFTL
732
Local INTO (DMA_DONE from DMA controller of PLX9080)
708a
708
Local R/W control signals
708b
Local Addr bus
708c
Local INTI #
708d
Local Data bus
708e
XSFR_DONE CHECKING LOGIC
1000
XSFR_DONE
1013
EVAL CONTROL LOGIC
1001
DATA_XSFER
736
Start EVAL
1014
DMA descriptor block
256x32 SRAM
A
DO
WE
DI
1002
DMA descriptor out
1046
1019
1020
ADDRESS DECODER
1005
1021
Write_Flag SEQUENCER
1006
1022
1023
1027
1028
1029
Control Register
1003
DO
WE
DI
WR_XSFR, RD_XSFR
1015
Set EVAL time
1041
EVAL TIMER
1004
EVAL
737
EVAL_DONE
1017
1016
SEM_F[redacted]
output e[redacted]
SEM_FPGA SPACE addr
738
Start Write_Flag
1018
1030
1031
LATCH
DI
DO
EN
1009
1032
1033
1010
SEM_FPGA low bank data bus
725
1024
1047
SEM_FPGA R/W CONTROL
1007
1048
1026
1025
1035
1036
1011
SEM_F[redacted]gh
bank dat[redacted]
726
1037
1038
F-WR
734
F-RD
735
Local Data Out
DEMUX and LATCH
108
1042
EVAL_DONE
1043
XSFR_DONE
1044
EVAL
1045
DMA descriptor out
1039
1012
1040
1034
701 and 707

FIG. 23

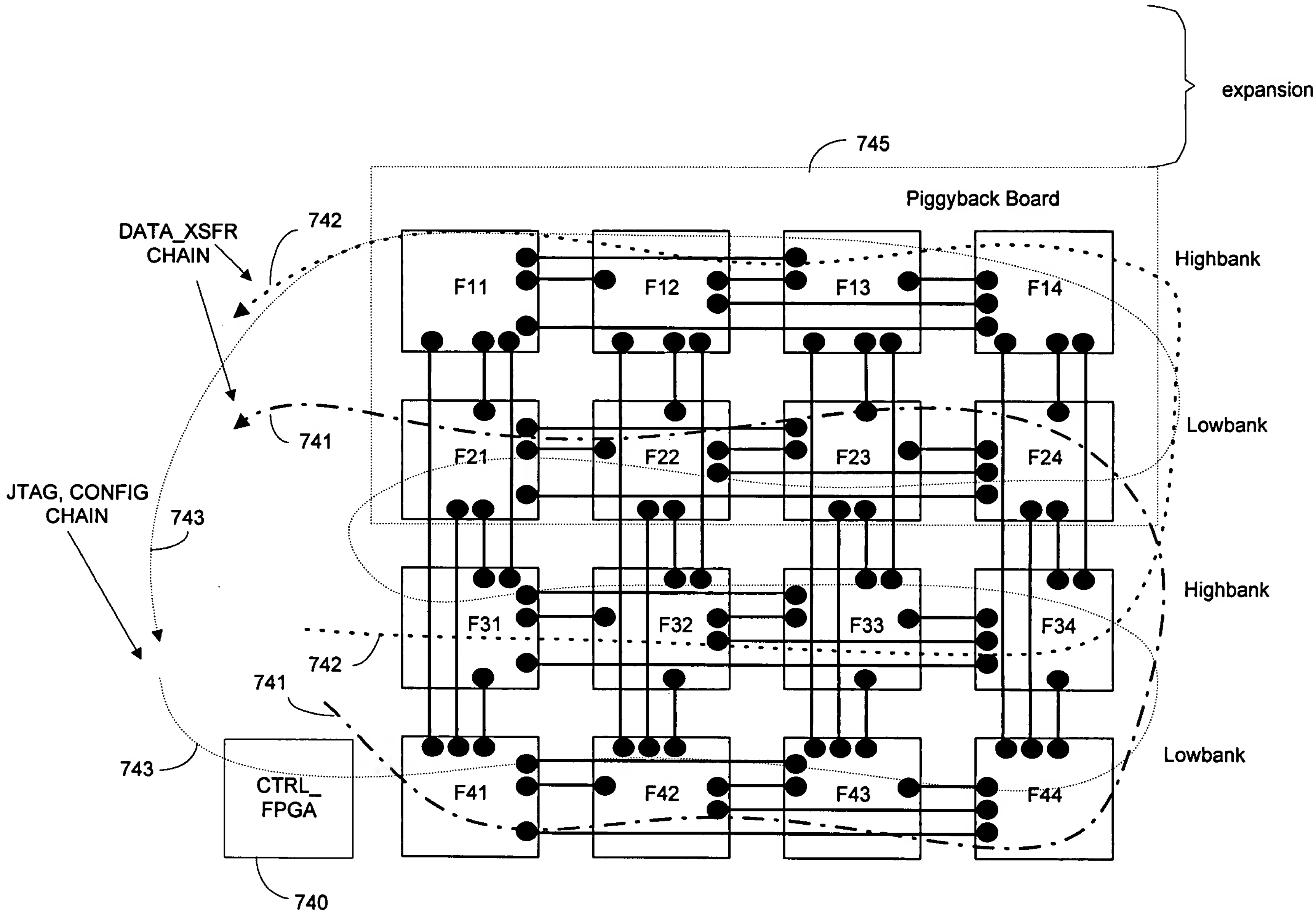

expansion
745
Piggyback Board
Highbank
Lowbank
Highbank
Lowbank
F11
F12
F13
F14
F21
F22
F23
F24
F31
F32
F33
F34
F41
F42
F43
F44
DATA_XSFR CHAIN
742
741
JTAG, CONFIG CHAIN
743
742
741
743
CTRL_ FPGA
740

FIG. 24

HARDWARE START-UP

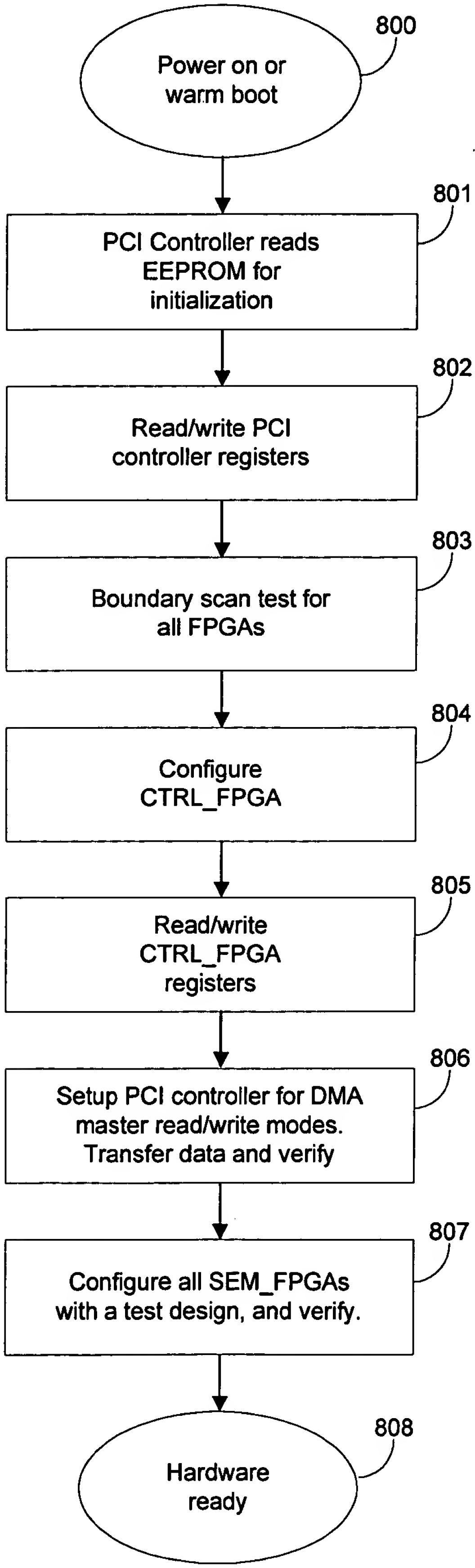


FIG. 25

```
module register (clock, reset, d, q);
input clock, d, reset;
output q;
reg q;

always@(posedge clock or negedge reset)
    if(~reset)
        q = 0;
    else
        q = d;

endmodule

module example;
    wire d1, d2, d3;
    wire q1, q2, q3;

    reg sigin;
    wire sigout;
    reg clk, reset;

    register reg1 (clk, reset, d1, q1);
    register reg2 (clk, reset, d2, q2);
    register reg3 (clk, reset, d3, q3);

    assign d1 = sigin ^ q3;
    assign d2 = q1 ^ q3;
    assign d3 = q2 ^ q3;
    assign sigout = q3;

    // a clock generator
    always
    begin
        clk = 0;
        #5;
        clk = 1;
        #5;
    end

    // a signal generator
    always
    begin
        #10;
        sigin = $random;
    end

    // initialization
    initial
    begin
        reset = 0;
        sigin = 0;
        #1;
        reset =1;
        #5;
        $monitor($time, " %b, %b", sigin, sigout);
        #1000 $finish;
    end
    end module
```

FIG. 26

CIRCUIT DIAGRAM

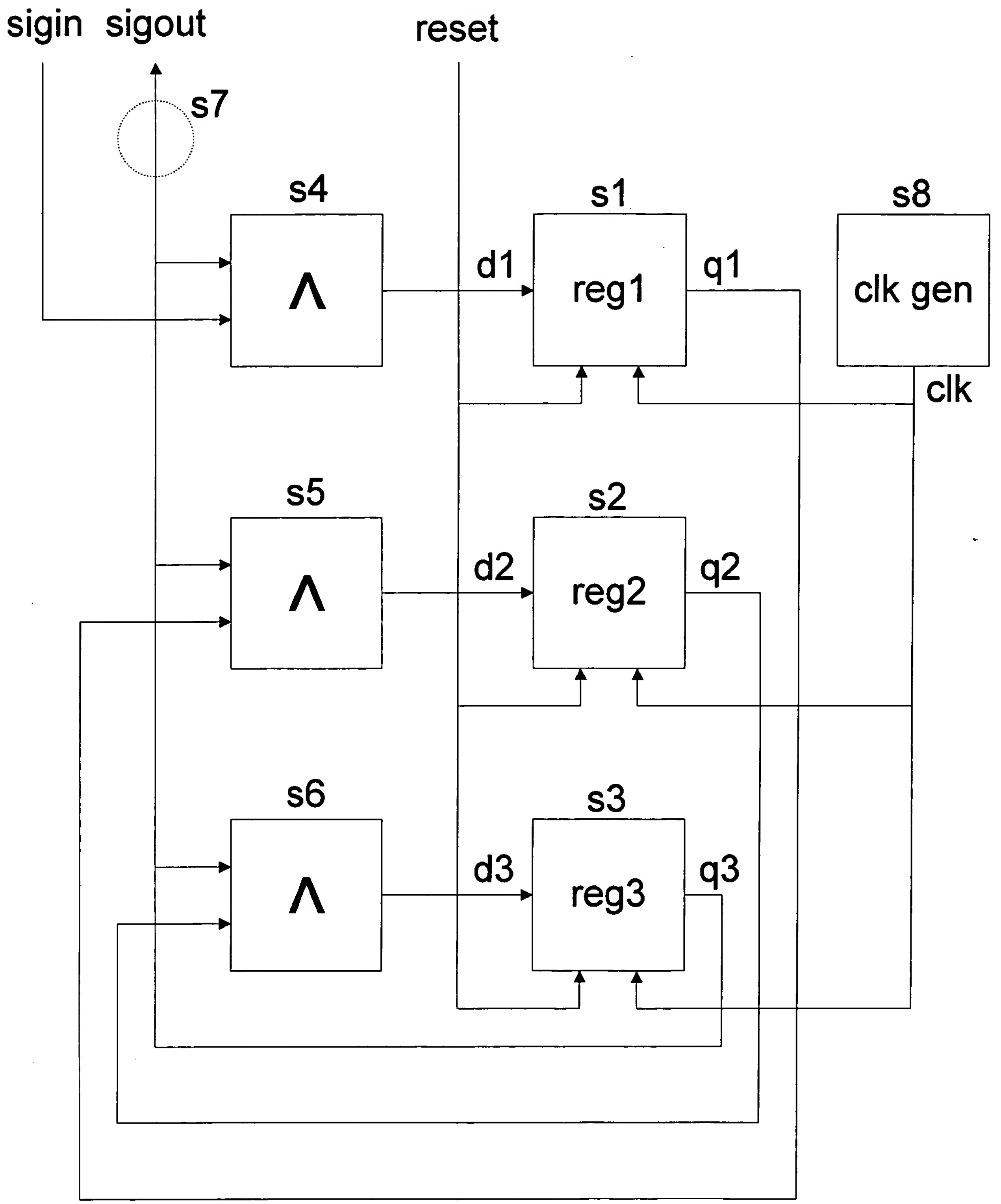


FIG. 27

```
module register (clock, reset, d, q);
input clock, d, reset;
output q;
reg q;

always@(postedge clock or negedge reset)              Register Definition
    if(~reset)                                         900
        q = 0
    else
        q = d;

endmodule

module example;
    wire d1, d2, d3;                  wire interconnection info
    ware q1, q2, q3;                  907

    reg sigin;                        Test-bench input -- 908
    wire sigout;                      Test-bench output -- 909
    reg clk, reset;

S1  register reg 1 (clk, reset, d1, q1);
S2  register reg 2 (clk, reset, d2, q2);    Register component
S3  register reg 3 (clk, reset, d3, q3);    901

S4  assign d1 = sigin ^ q3;
S5  assign d2 = q1 ^ 3;               Combinational component
S6  assign d3 = q2 ^ q3;              902
S7  assign signout = q3;

        // a clock generator
        always
        begin
S8          clk = 0;                  Clock component
            #5;                       903
            clk = 1;
            #5;
        end

        // a signal generator
        always
        begin
S9          #10;                      Test-bench component (Driver)
            sigin = $random;          904
        end

        // initialization
        initial
        begin
            reset = 0;
S10         sigin = 0;                Test-bench component (initialization)
            #1;                       905
S11         reset = 1;
            #5;
S12         $monitor($time, "%b, %b", sigin, sigout);   Test-bench component (monitor)
            #1000 $finish;                              906
        end
        end module
```

FIG. 28

SIGNAL NETWORK ANALYSIS

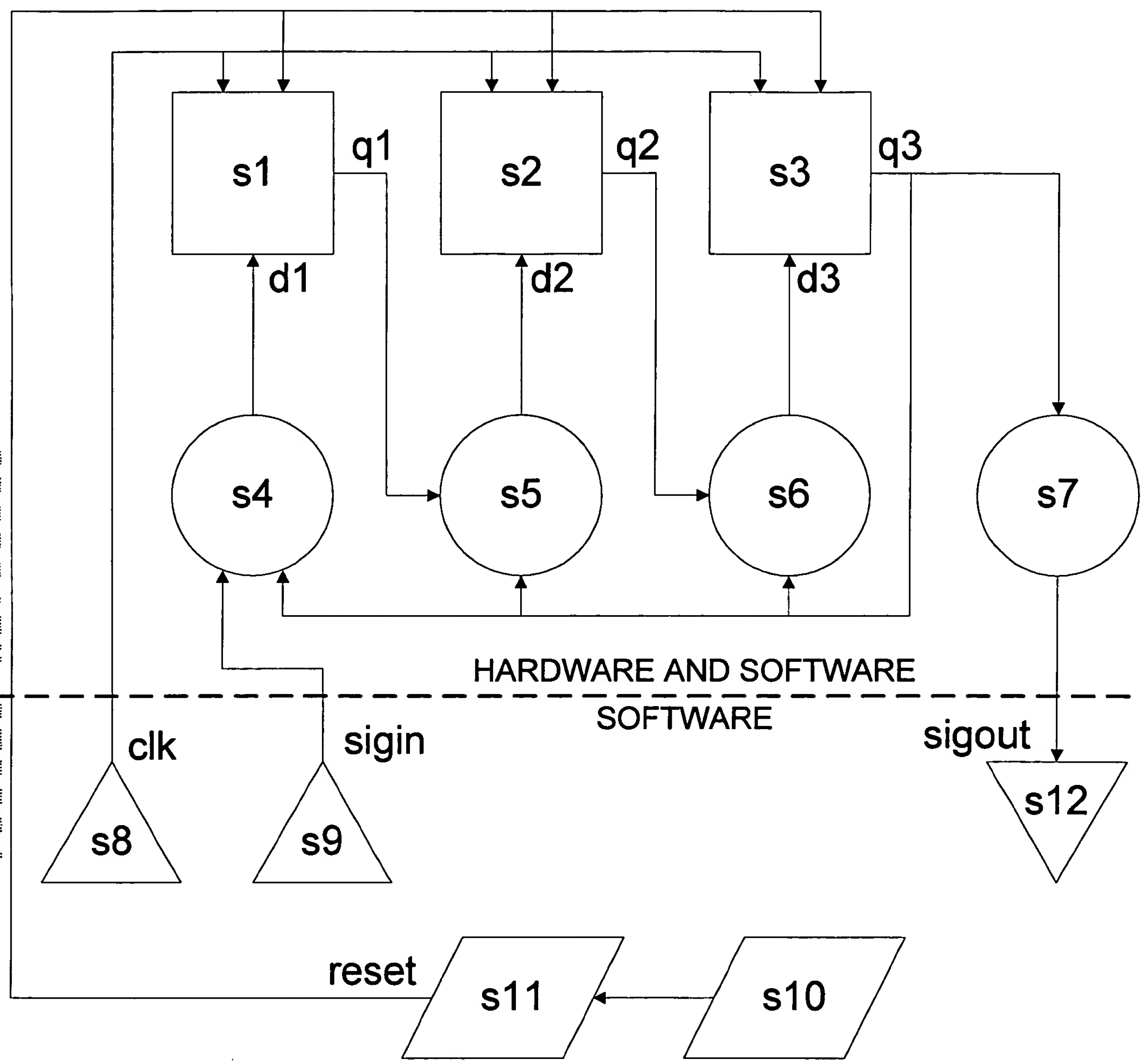


FIG. 29

SOFTWARE/HARDWARE PARTITION RESULT

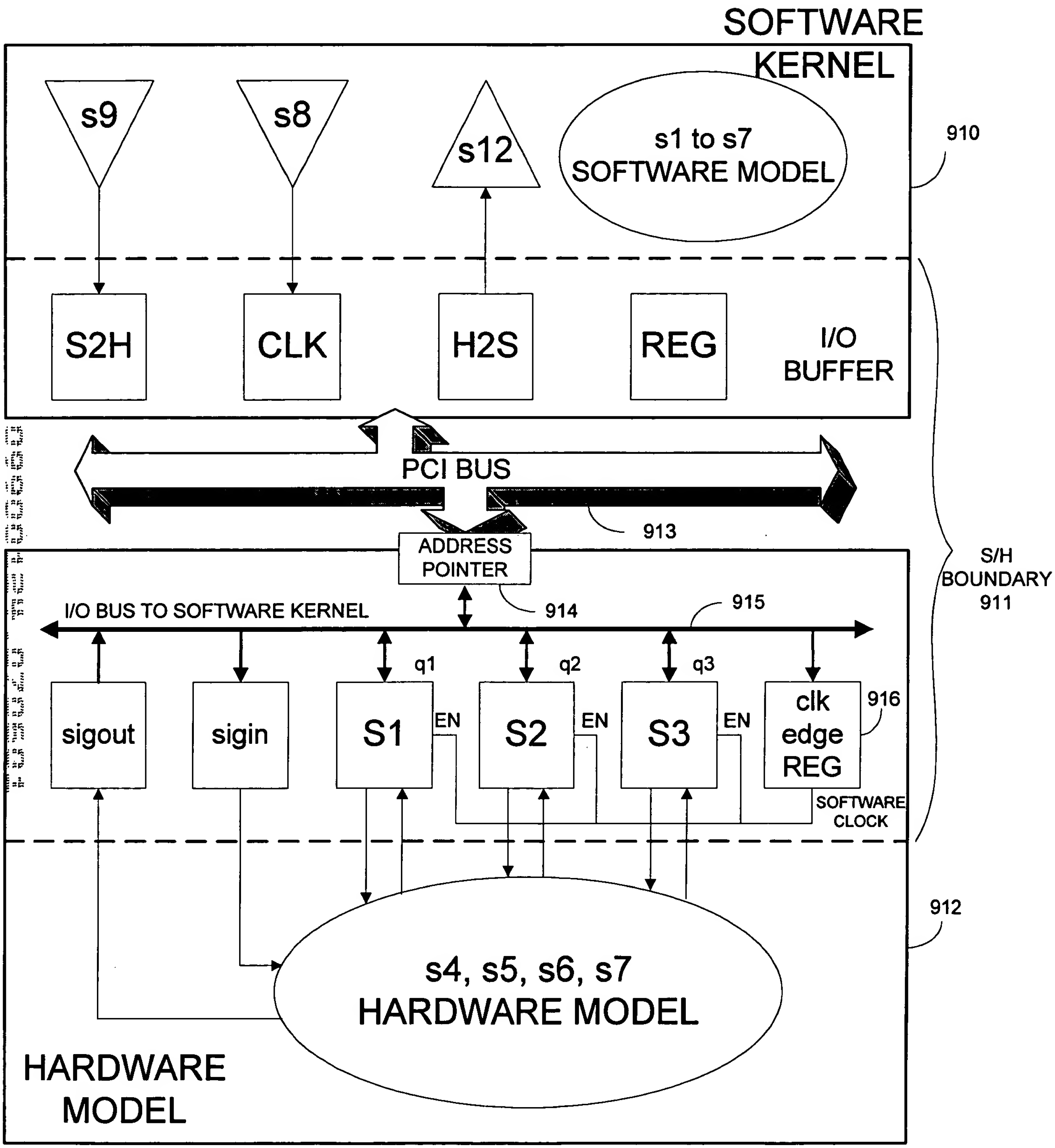


FIG. 30

HARDWARE MODEL

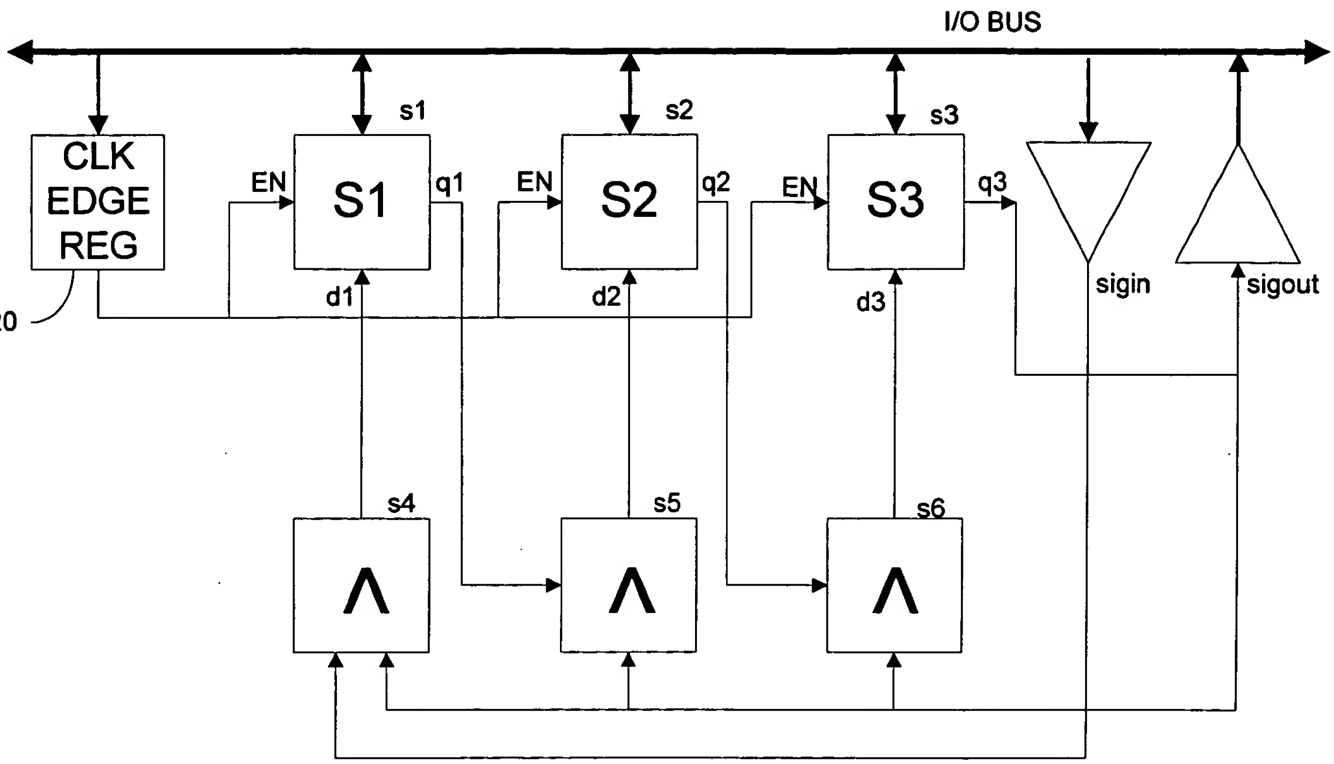
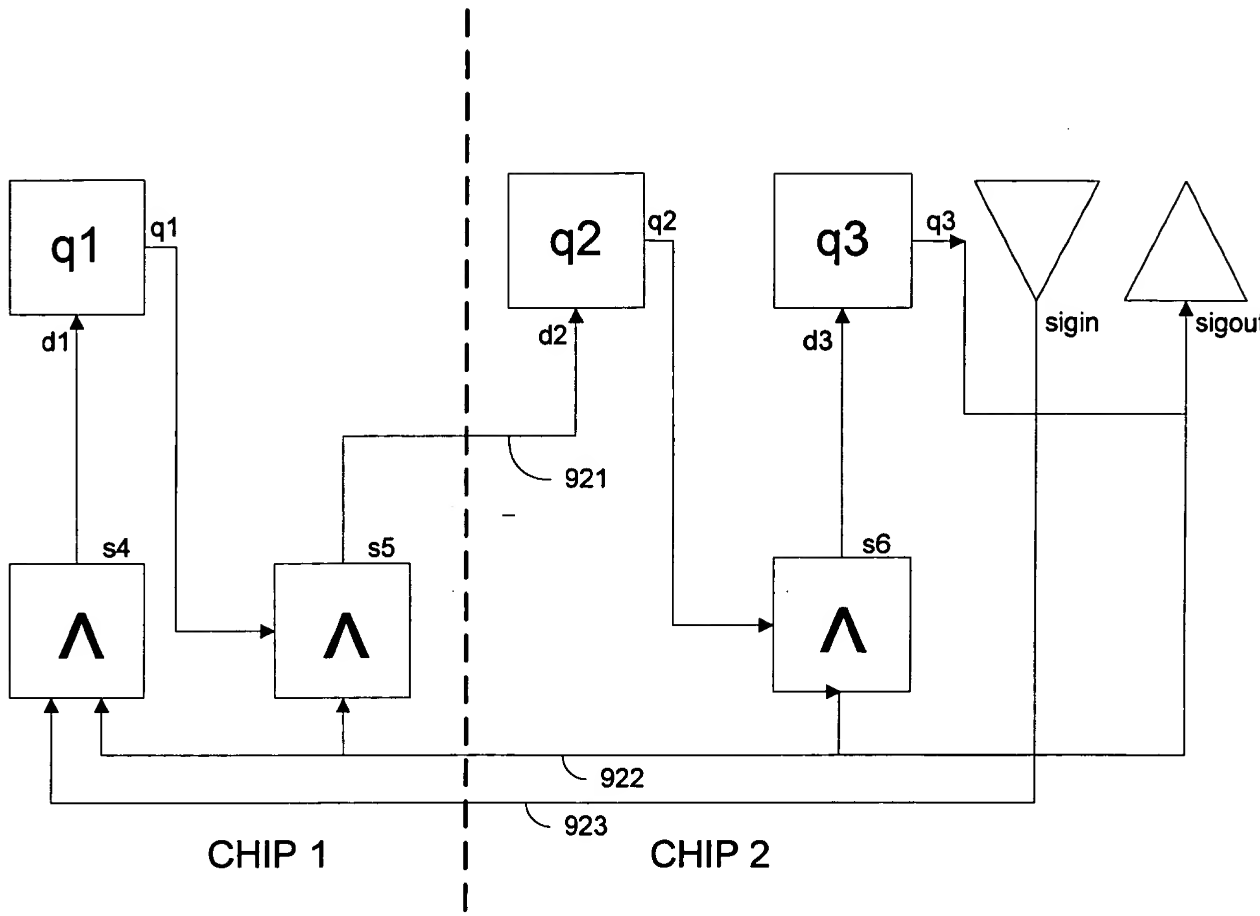


FIG. 31

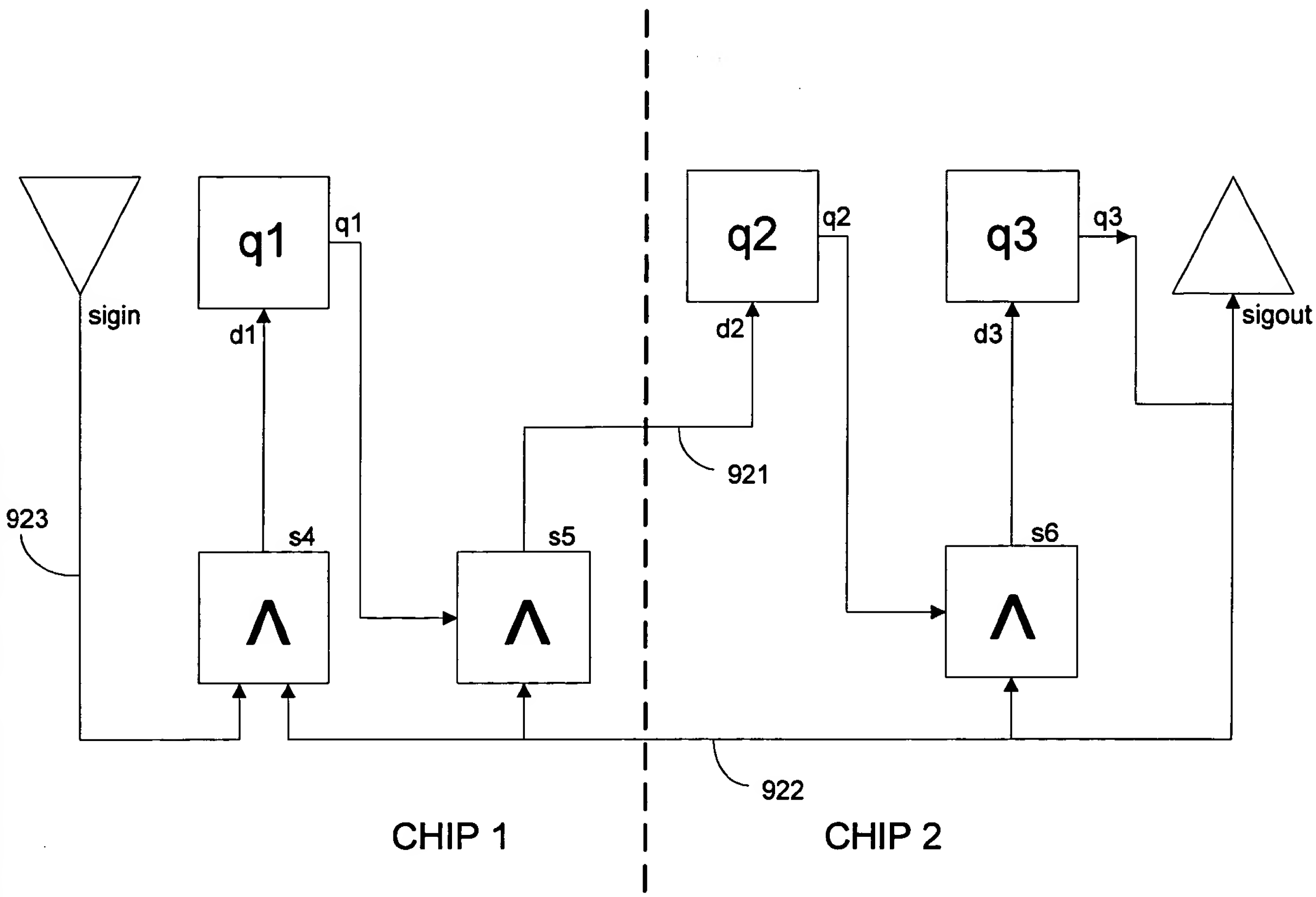
PARTITION RESULT #1



(IGNORE I/O AND CLOCK EDGE REGISTER)

FIG. 32

PARTITION RESULT #2



(IGNORE I/O AND CLOCK EDGE REGISTER)

FIG. 33

LOGIC PATCHING

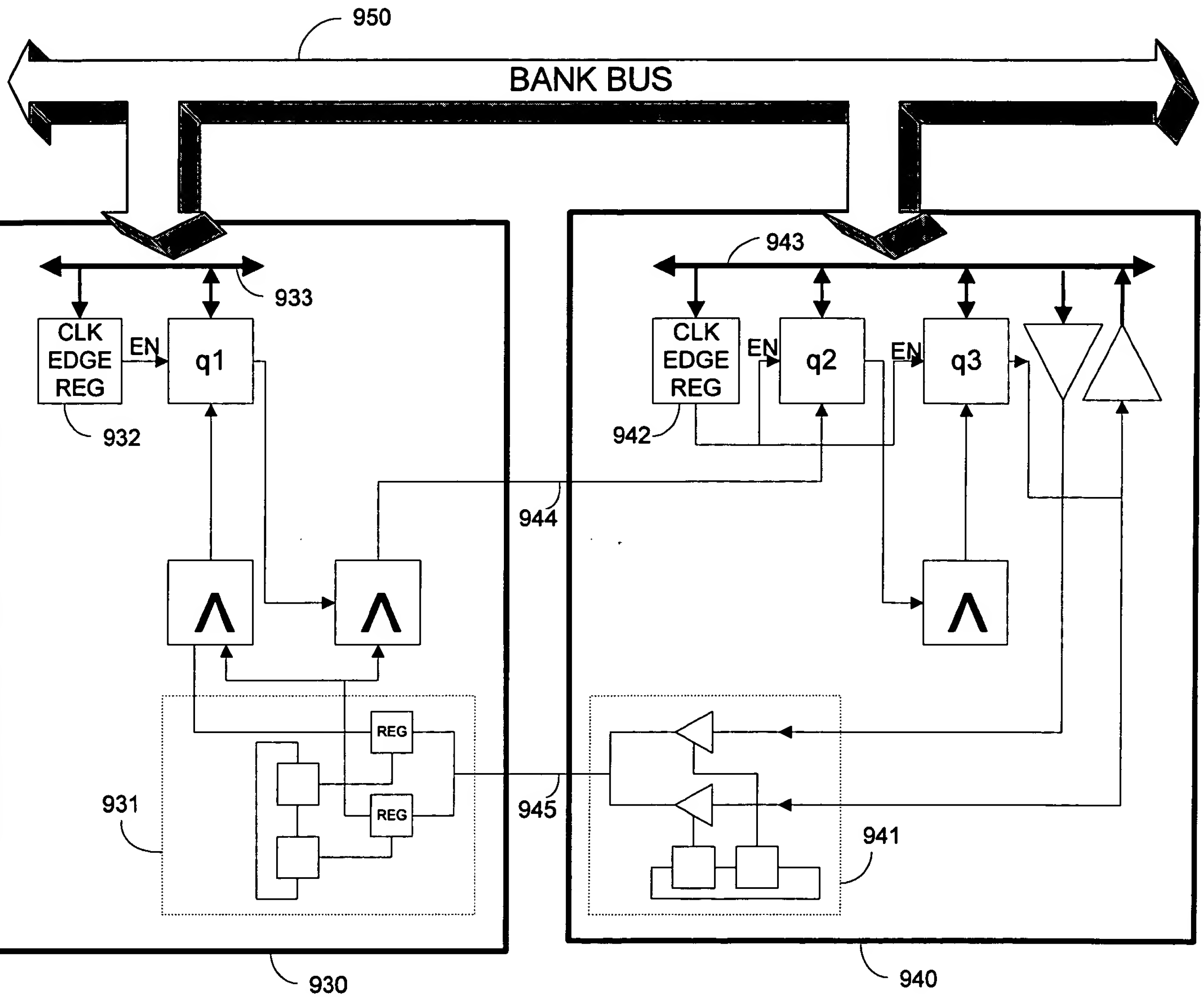


FIG. 34

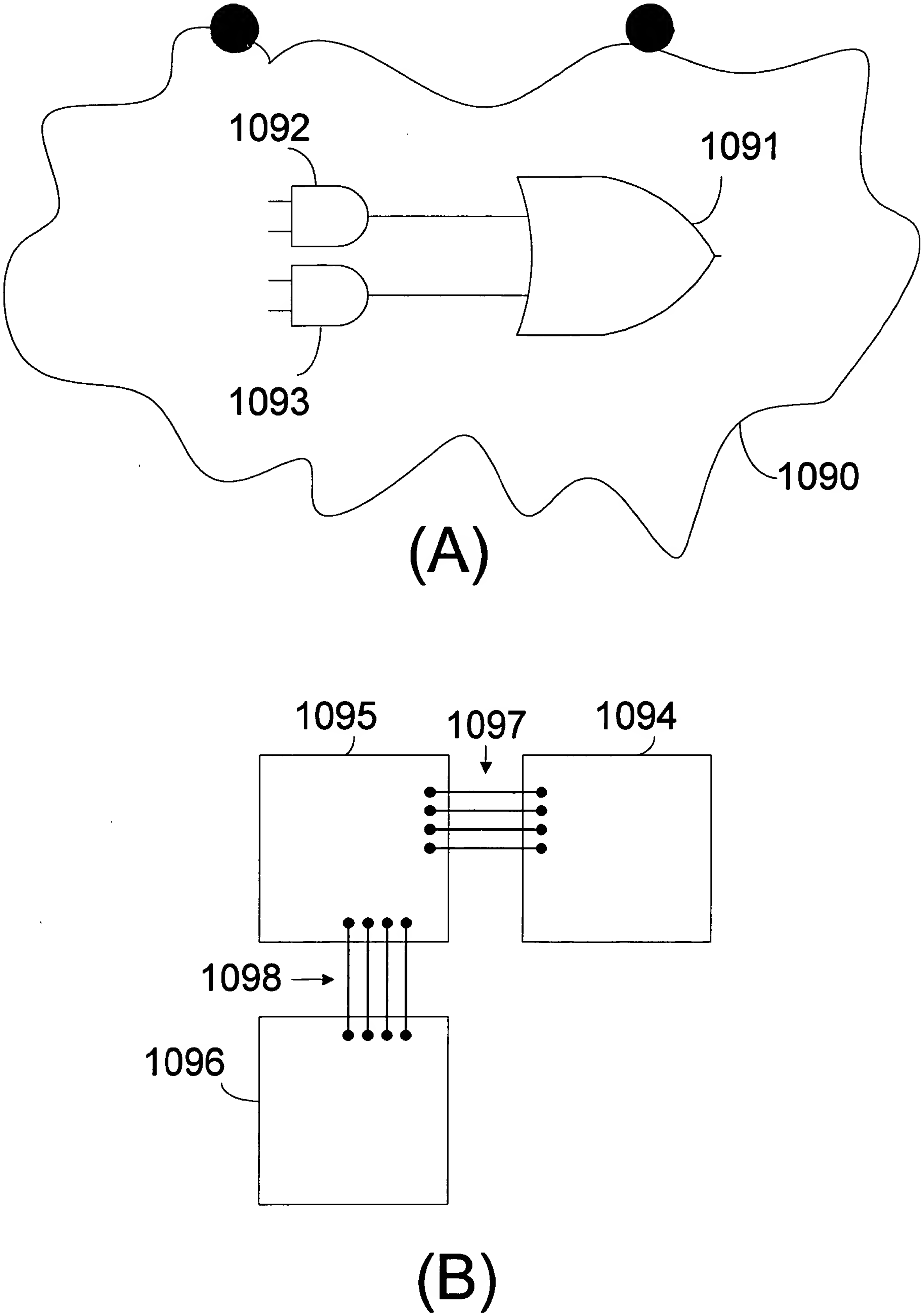
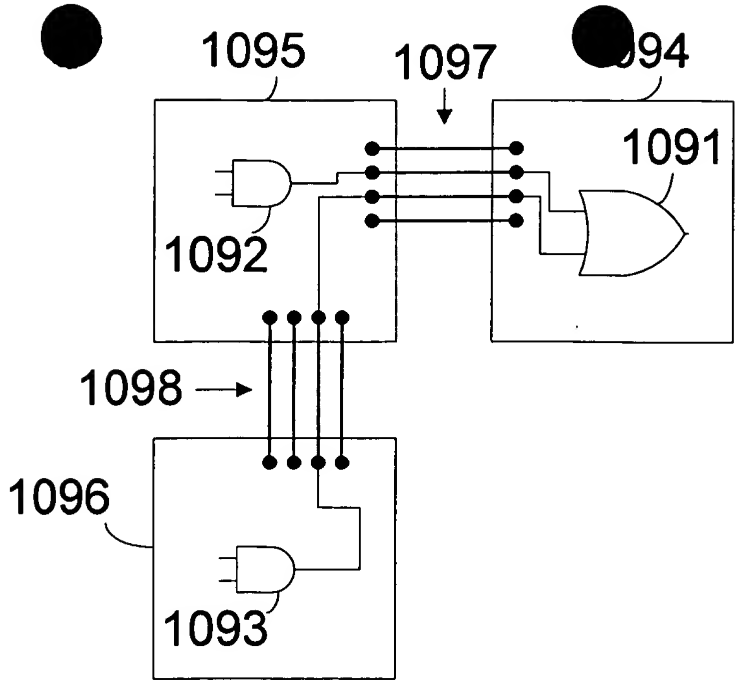
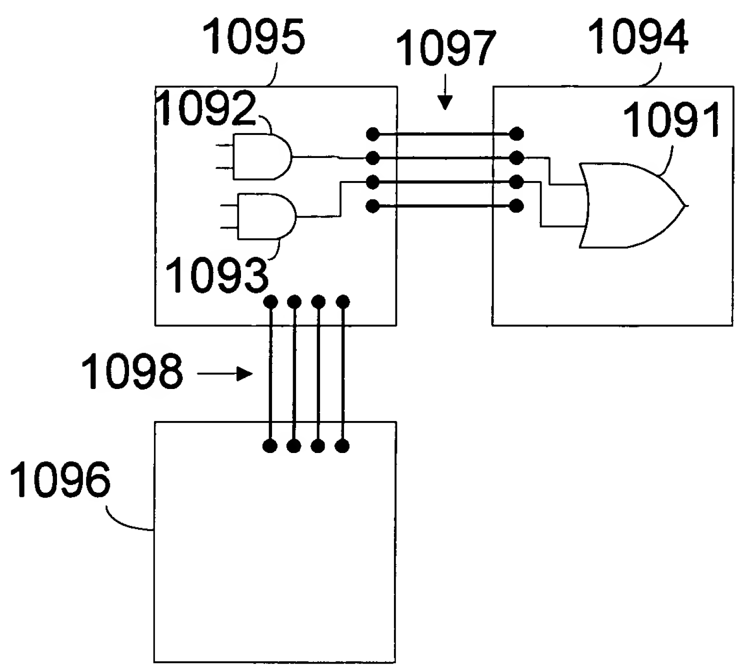


FIG. 35


1095
1097
094
1091
1092
1098
1096
1093

(C)

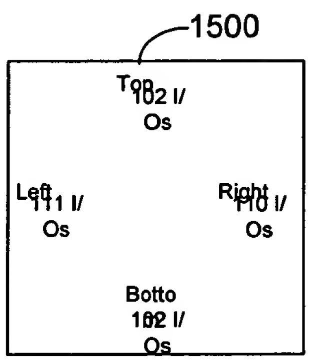

1095
1097
1094
1092
1091
1093
1098
1096

(D)

FIG. 35

I/O PIN OVERVIEW OF FPGA LOGIC DEVICE

FPGA : 10K130V, 10K250V with 599-pin PGA package



425 Interconnect I/O pins

45 Dedicated I/O pins:

GCLK, BUS[31..0], F_RD,
F_WR, DATAXSFR, SHIFTIN,
SPACE[2..0], SEL_EVAL,
DEV_OE, EVREQ_N,
DEV_CLRN

FIG. 36

FPGA INTERCONNECT BUSES

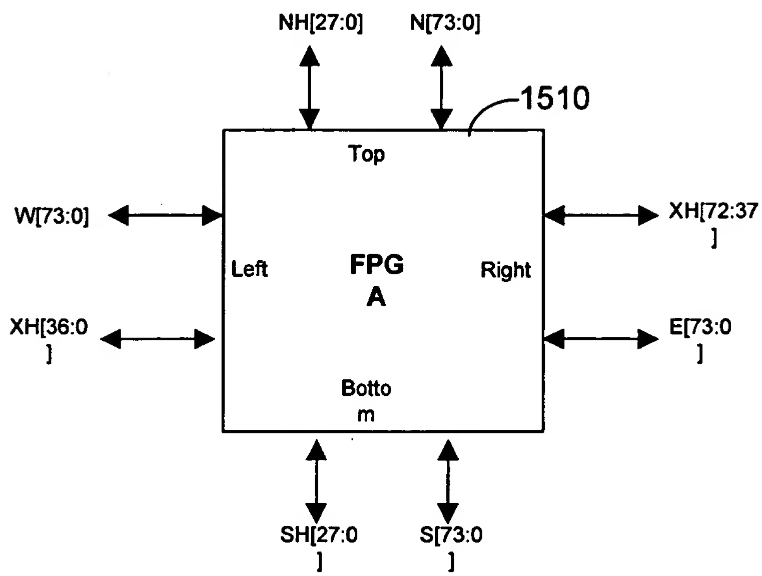


FIG. 37

BOARD CONNECTION - SIDE VIEW

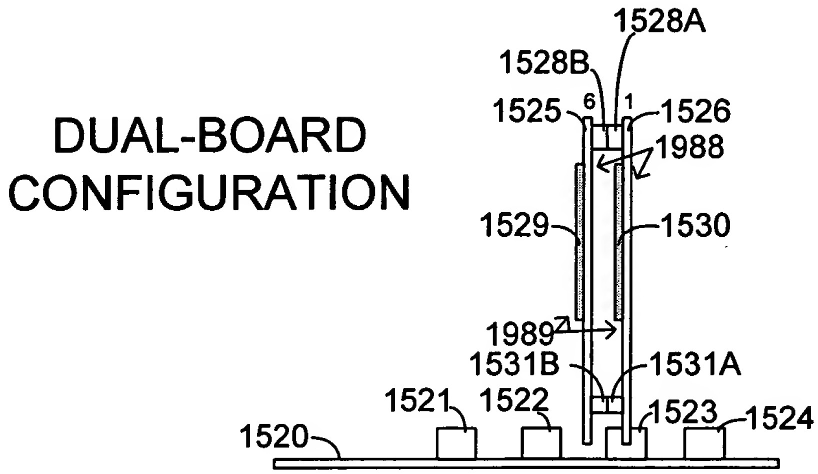


FIG. 38(A)

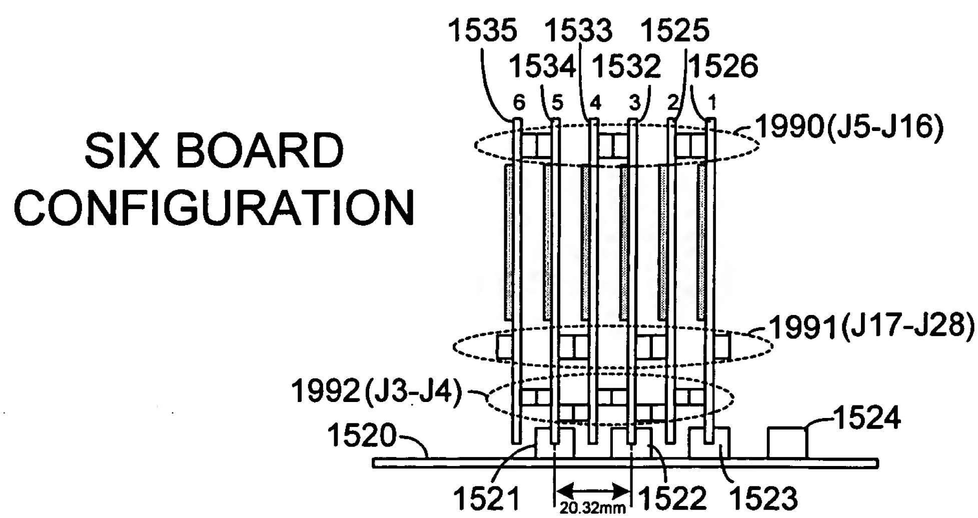


FIG. 38(B)

SIX-BOARD CONFIGURATION
DIRECT-NEIGHBOR AND ONE-HOP FPGA ARRAY – X TORUS, Y MESH

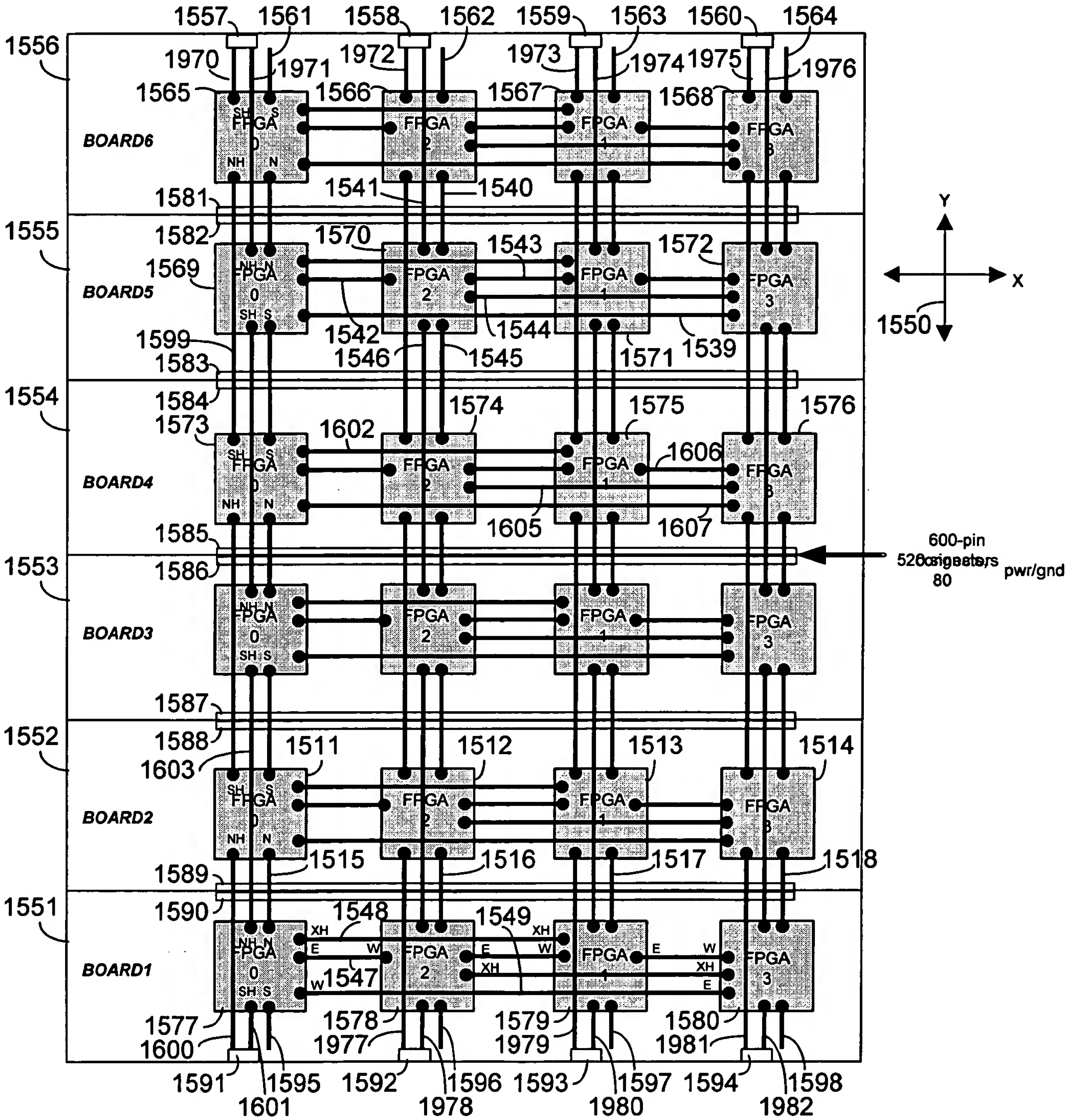


FIG. 39

FPGA ARRAY CONNECTION BETWEEN BOARDS

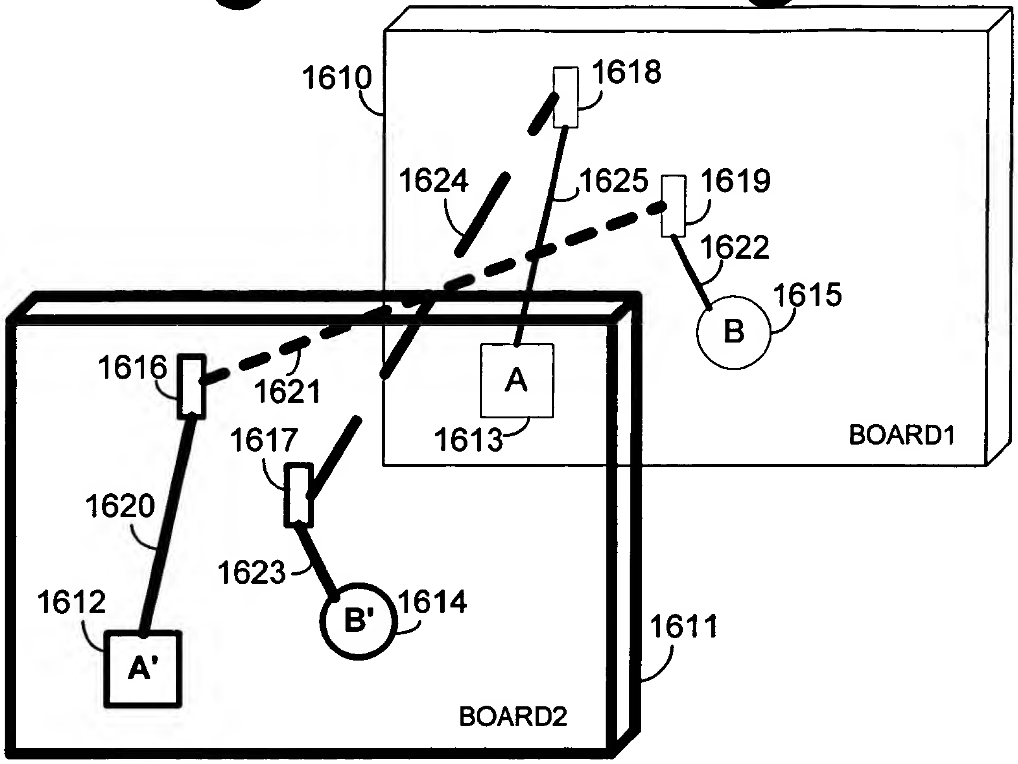


FIG. 40(A)

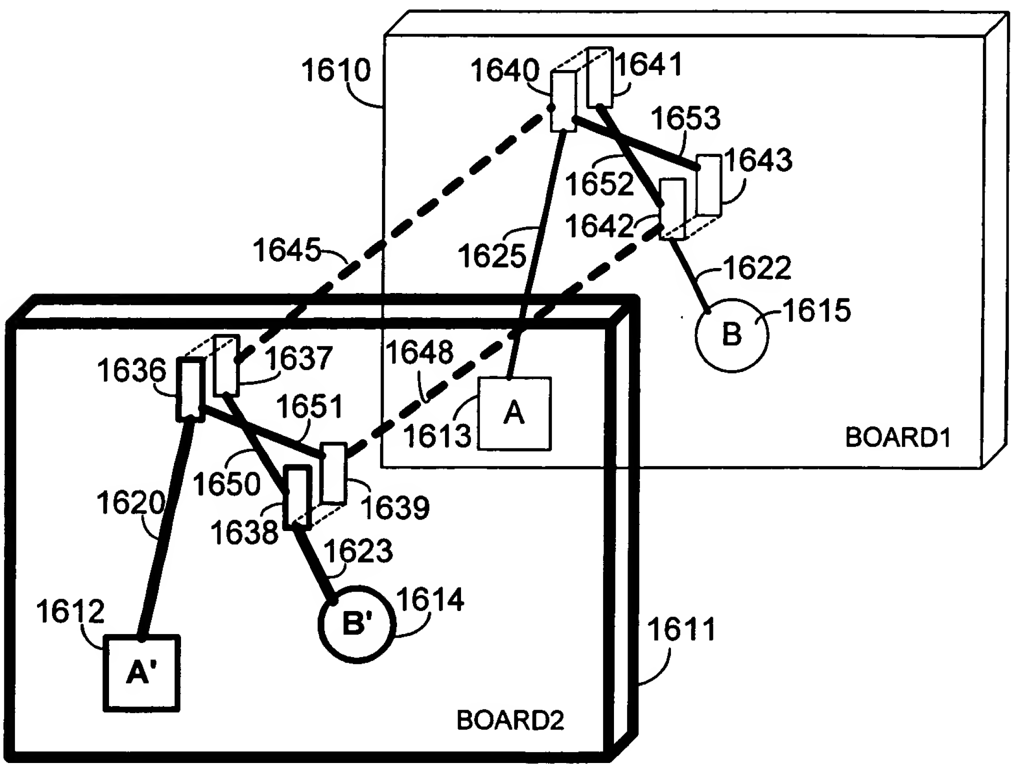


FIG. 40(B)

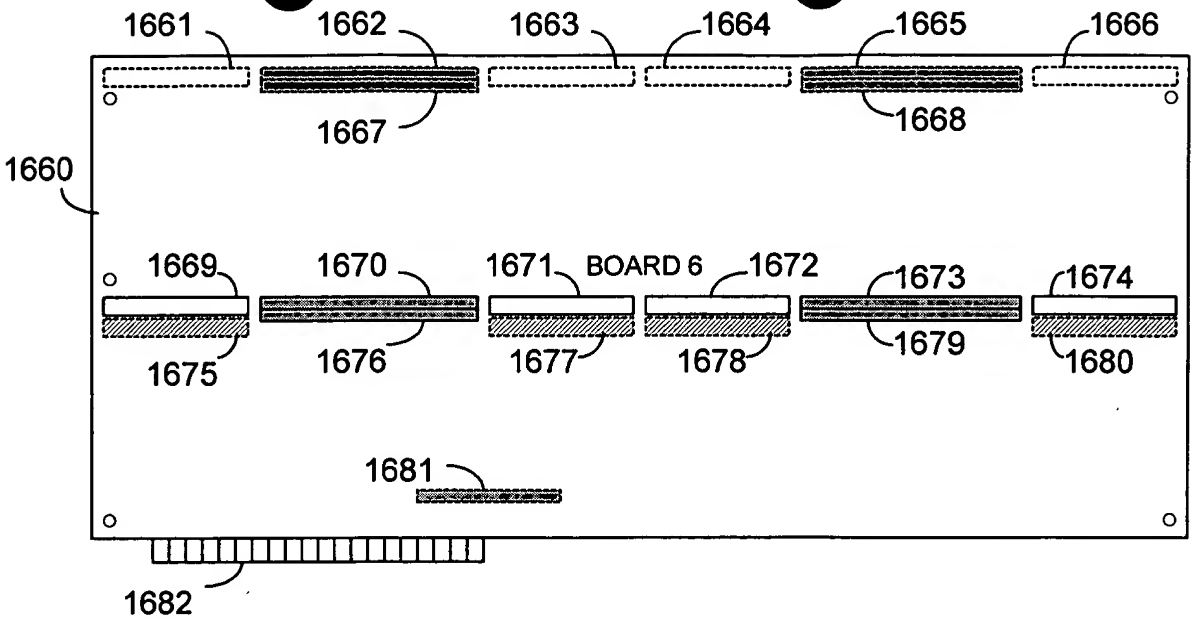


FIG. 41(A)

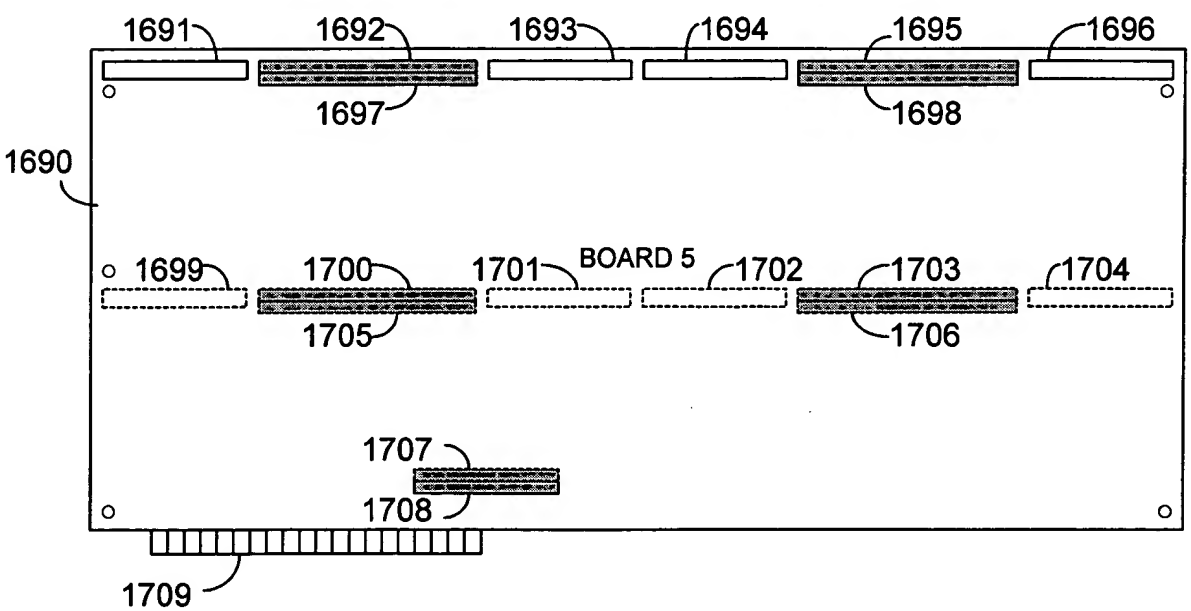


FIG. 41(B)

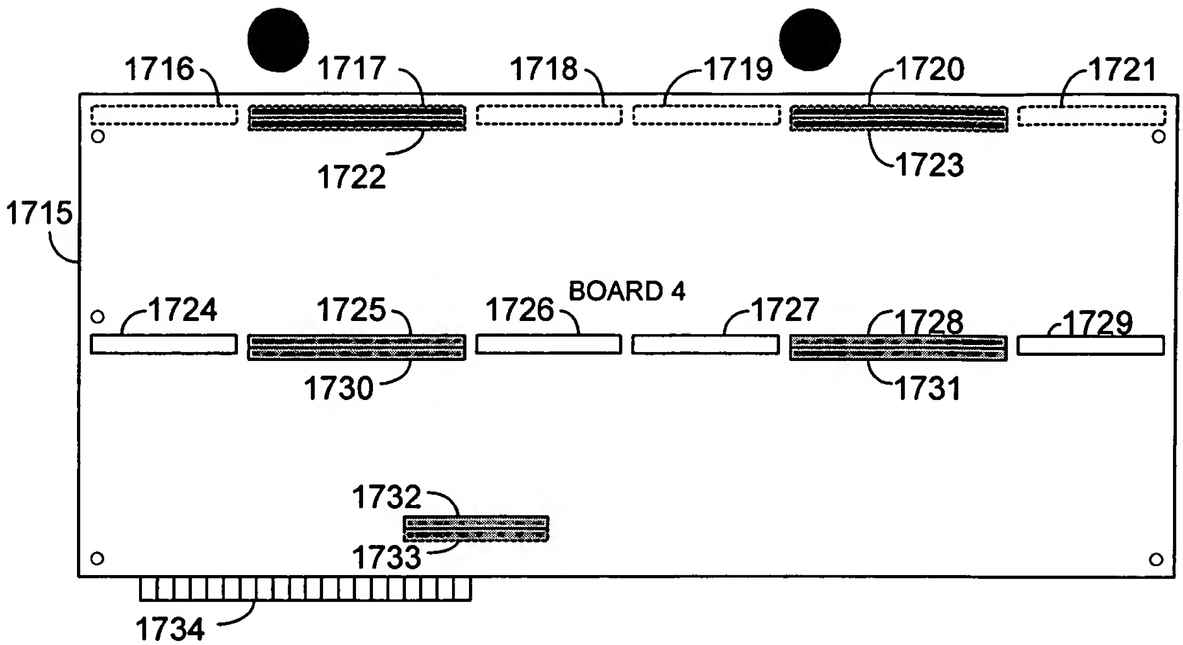


FIG. 41(C)

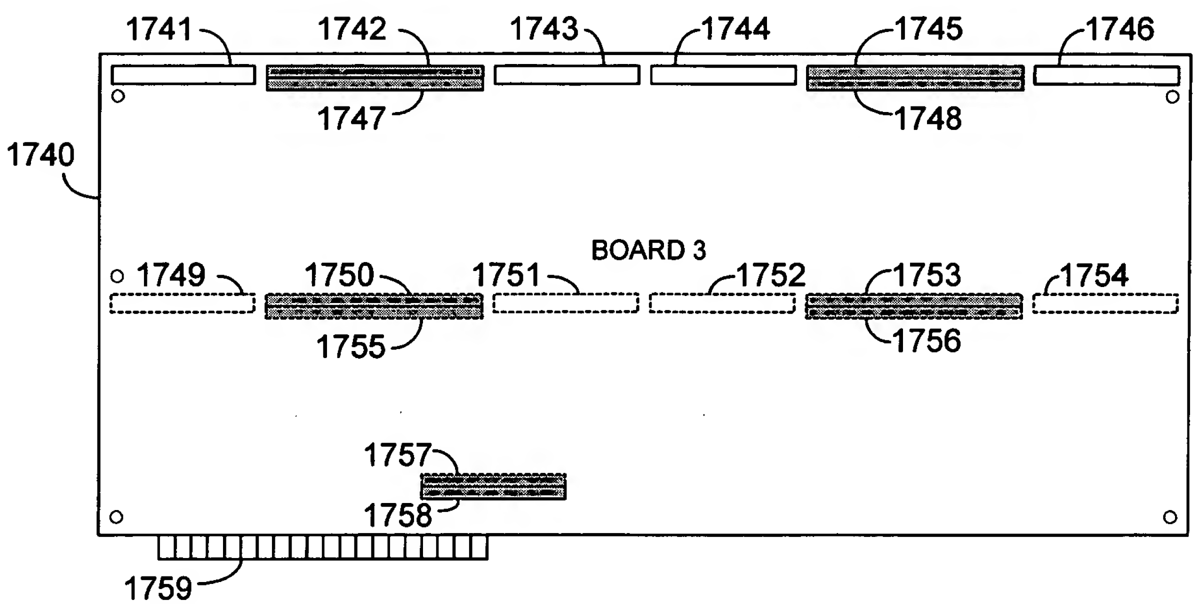


FIG. 41(D)

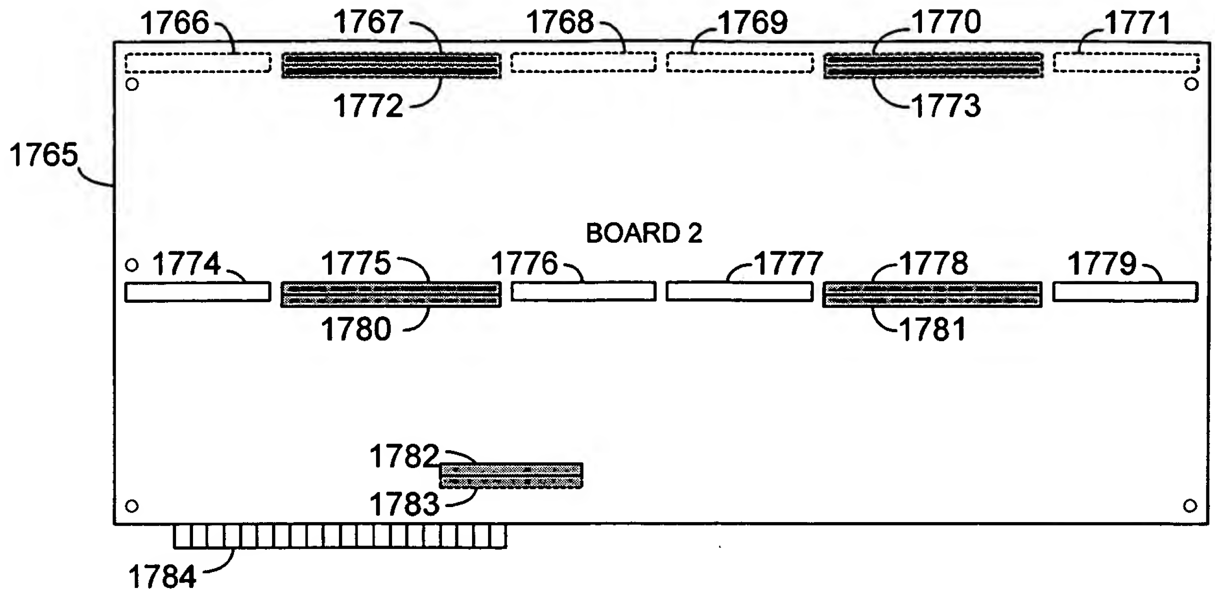


FIG. 41(E)

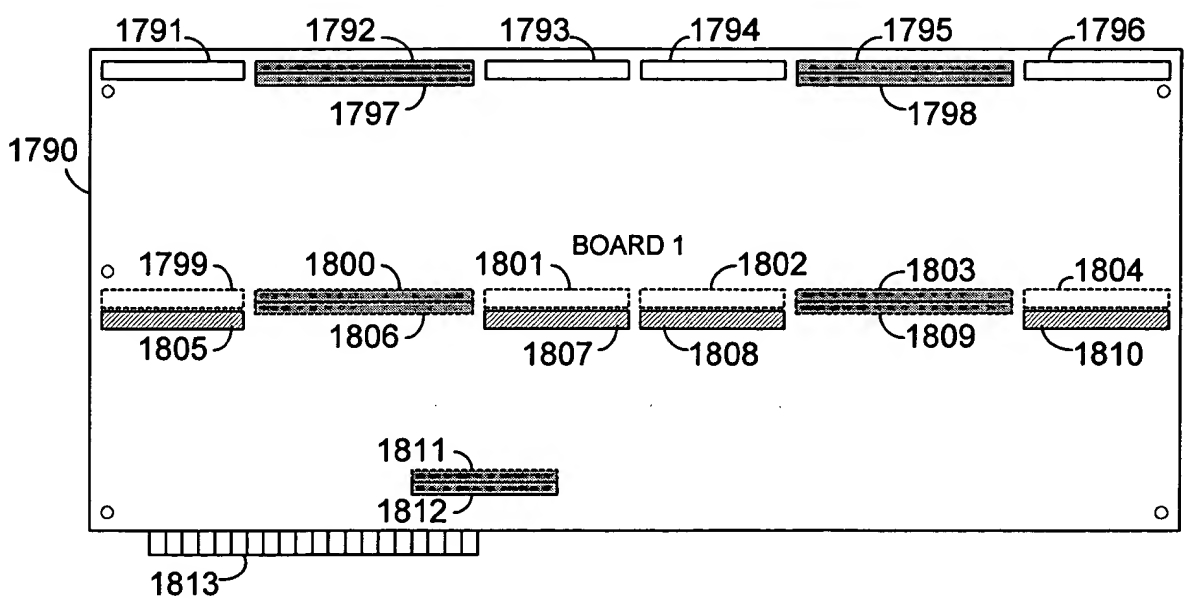


FIG. 41(F)

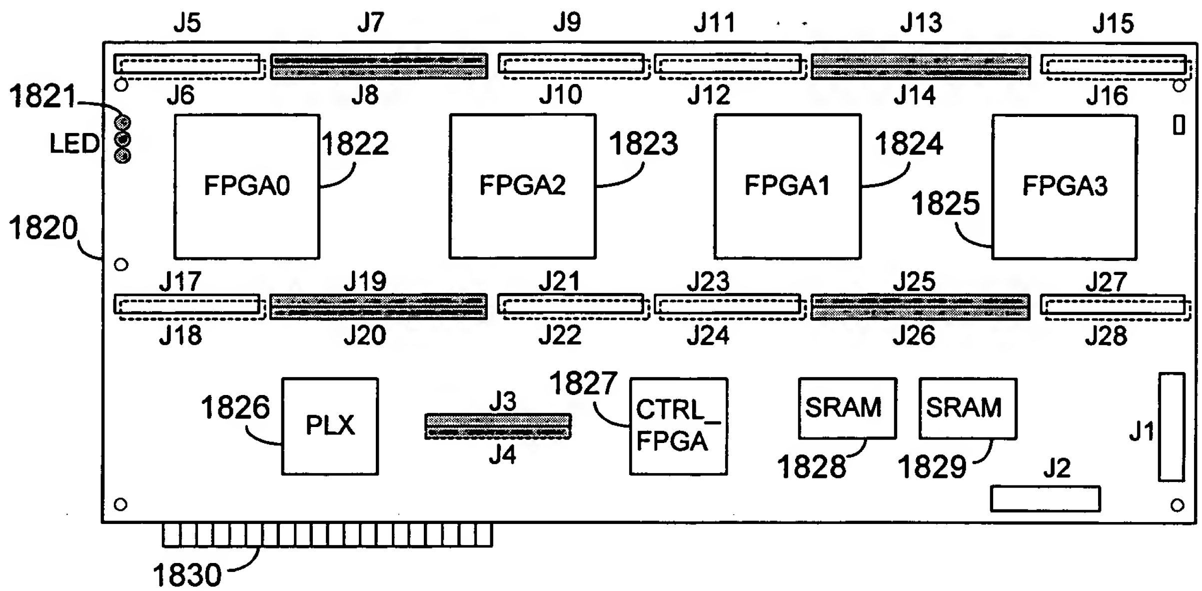

J5
J7
J9
J11
J13
J15
J6
J8
J10
J12
J14
J16
1821
LED
FPGA0
1822
FPGA2
1823
FPGA1
1824
1825
FPGA3
1820
J17
J19
J21
J23
J25
J27
J18
J20
J22
J24
J26
J28
1826
PLX
J3
J4
1827
CTRL_
FPGA
SRAM
SRAM
1828
1829
J1
J2
1830

FIG. 42

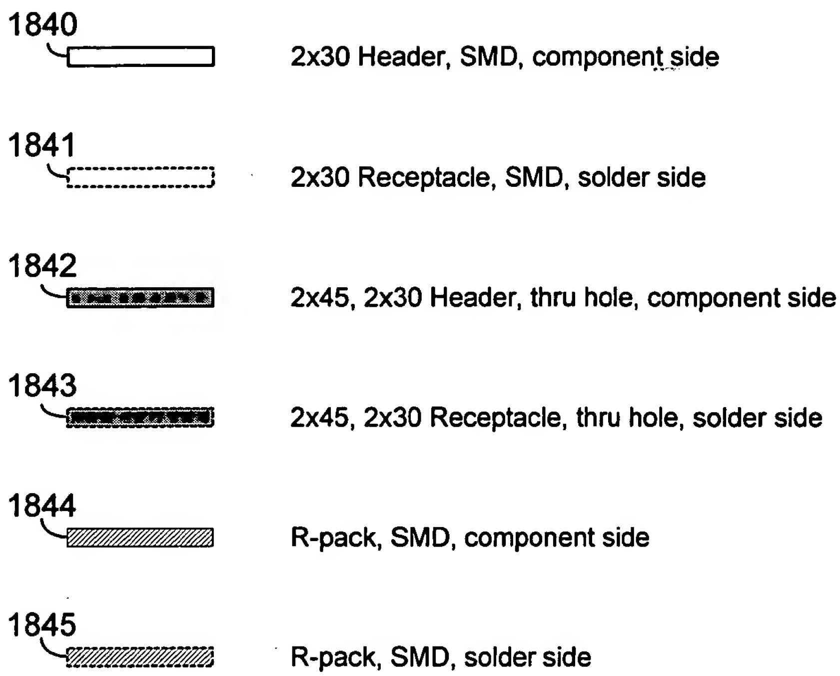

1840
2x30 Header, SMD, component side
1841
2x30 Receptacle, SMD, solder side
1842
2x45, 2x30 Header, thru hole, component side
1843
2x45, 2x30 Receptacle, thru hole, solder side
1844
R-pack, SMD, component side
1845
R-pack, SMD, solder side

FIG. 43

TWO-BOARD CONFIGURATION

DIRECT-NEIGHBOR AND ONE-HOP FPGA ARRAY – X TORUS, Y MESH

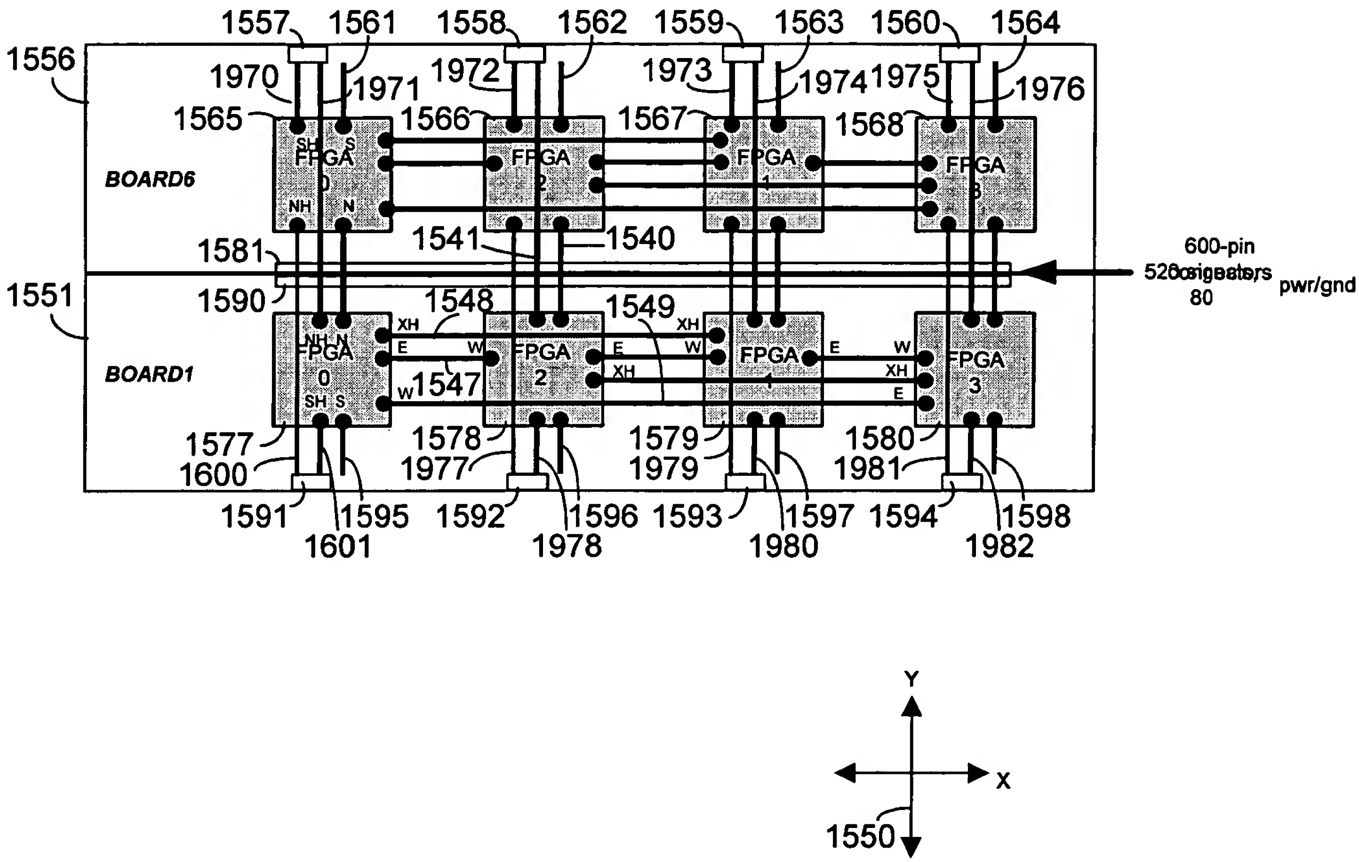


FIG. 44

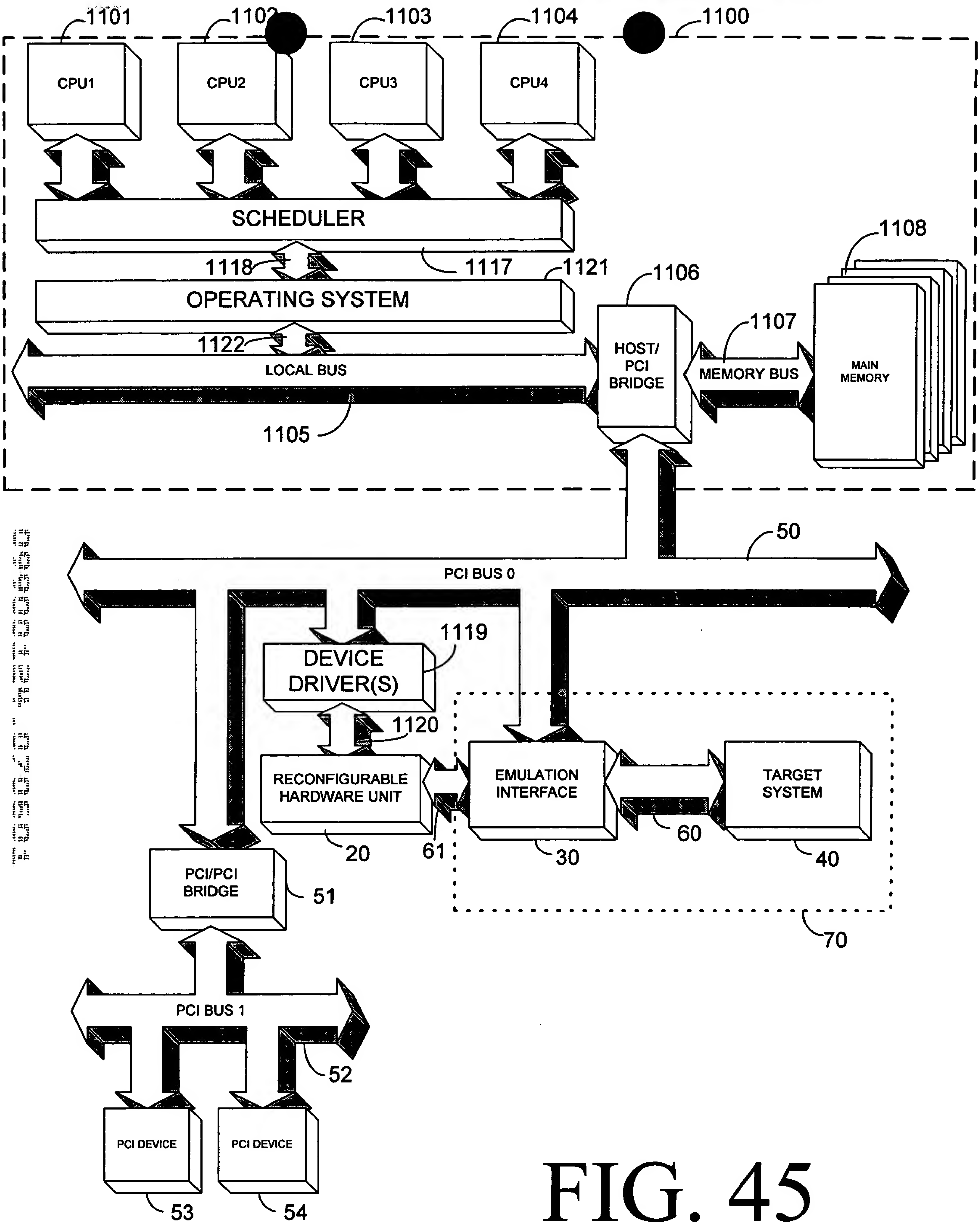
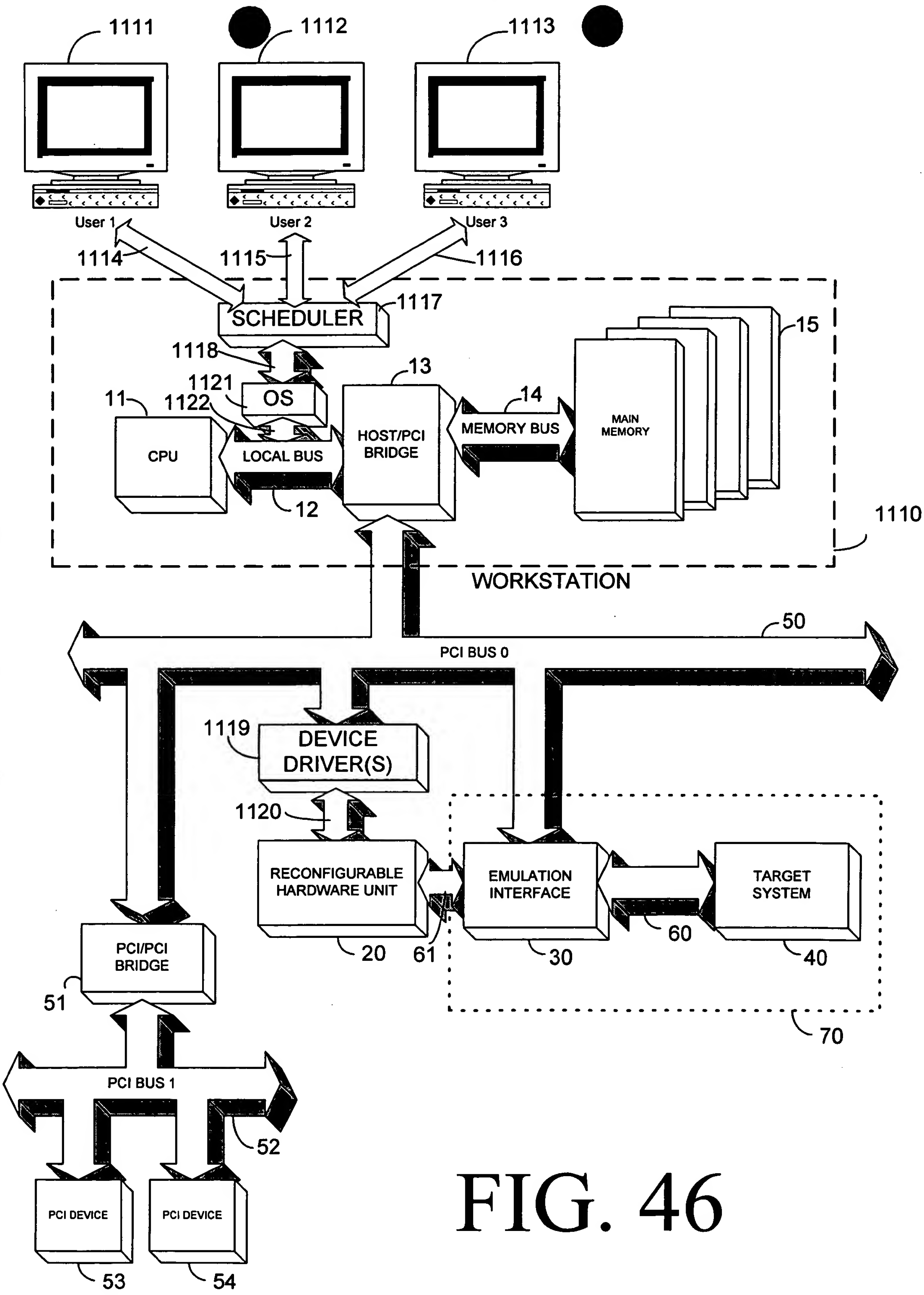

1101
1102
1103
1104
1100
CPU1
CPU2
CPU3
CPU4
SCHEDULER
1118
1117
1121
OPERATING SYSTEM
1106
1108
1122
LOCAL BUS
HOST/
PCI
BRIDGE
1107
MEMORY BUS
MAIN
MEMORY
1105
50
PCI BUS 0
1119
DEVICE
DRIVER(S)
1120
RECONFIGURABLE
HARDWARE UNIT
EMULATION
INTERFACE
TARGET
SYSTEM
60
20
61
30
40
PCI/PCI
BRIDGE
51
70
PCI BUS 1
52
PCI DEVICE
PCI DEVICE
53
54

FIG. 45



1111
1112
1113
User 1
User 2
User 3
1114
1115
1116
SCHEDULER
1117
1118
15
1121
OS
13
11
1122
14
MEMORY BUS
MAIN MEMORY
CPU
LOCAL BUS
HOST/PCI BRIDGE
12
1110
WORKSTATION
50
PCI BUS 0
1119
DEVICE DRIVER(S)
1120
RECONFIGURABLE HARDWARE UNIT
EMULATION INTERFACE
TARGET SYSTEM
60
20
61
30
40
PCI/PCI BRIDGE
51
70
PCI BUS 1
52
PCI DEVICE
PCI DEVICE
53
54

FIG. 46

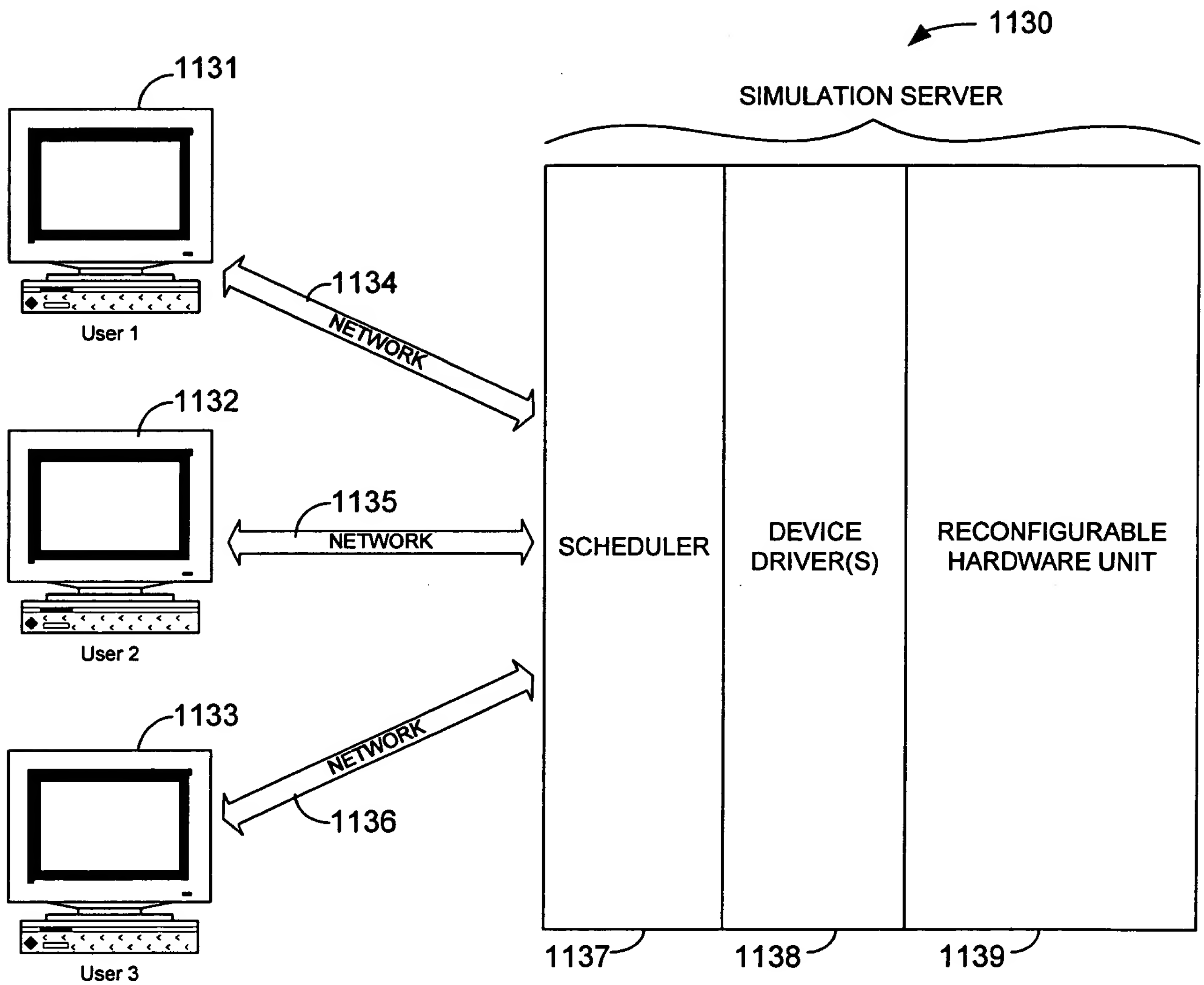

1130
SIMULATION SERVER
1131
User 1
1134
NETWORK
1132
User 2
1135
NETWORK
1133
User 3
NETWORK
1136
SCHEDULER
DEVICE DRIVER(S)
RECONFIGURABLE HARDWARE UNIT
1137
1138
1139

FIG. 47

SIMULATION SERVER ARCHITECTURE

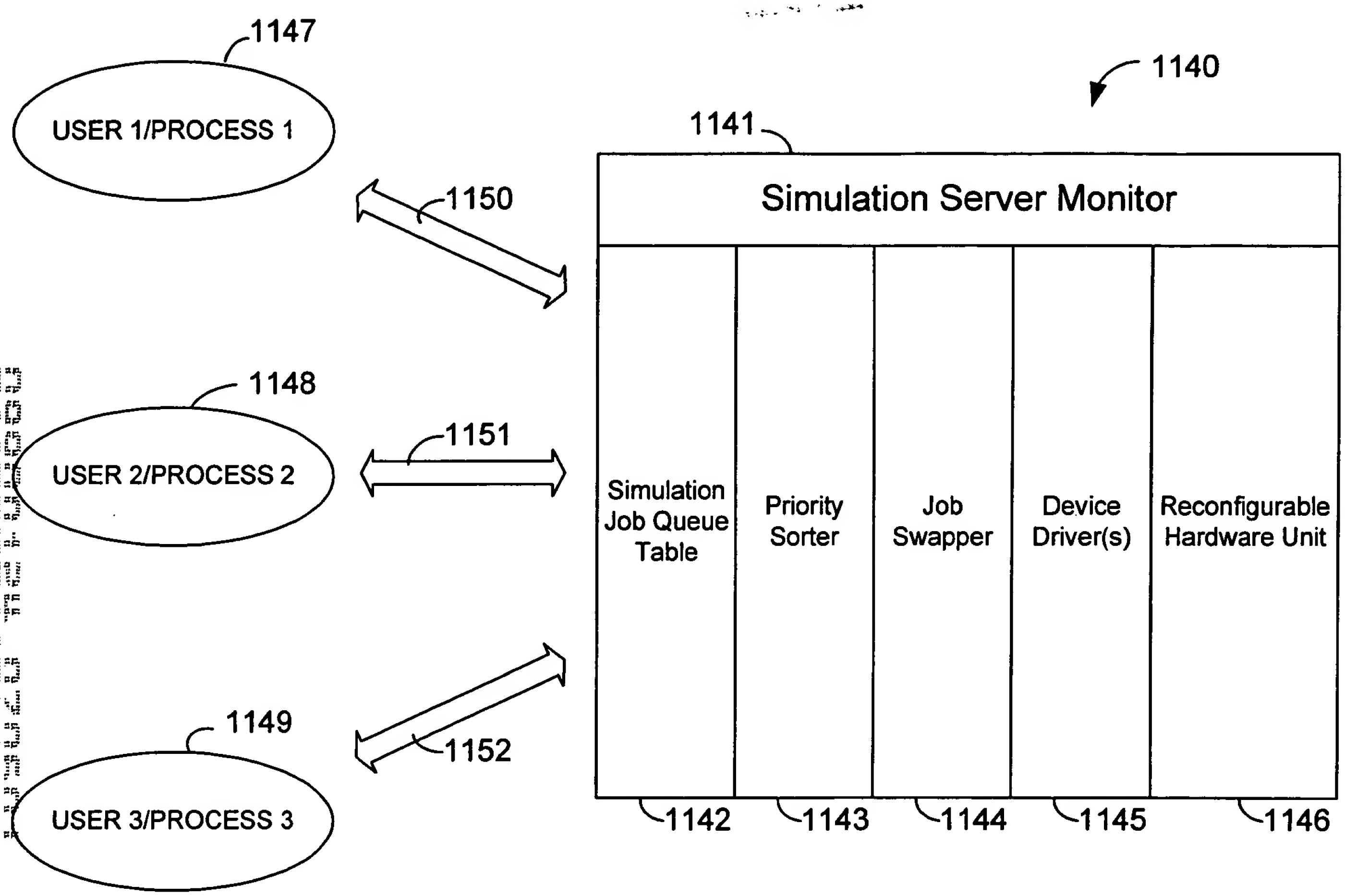
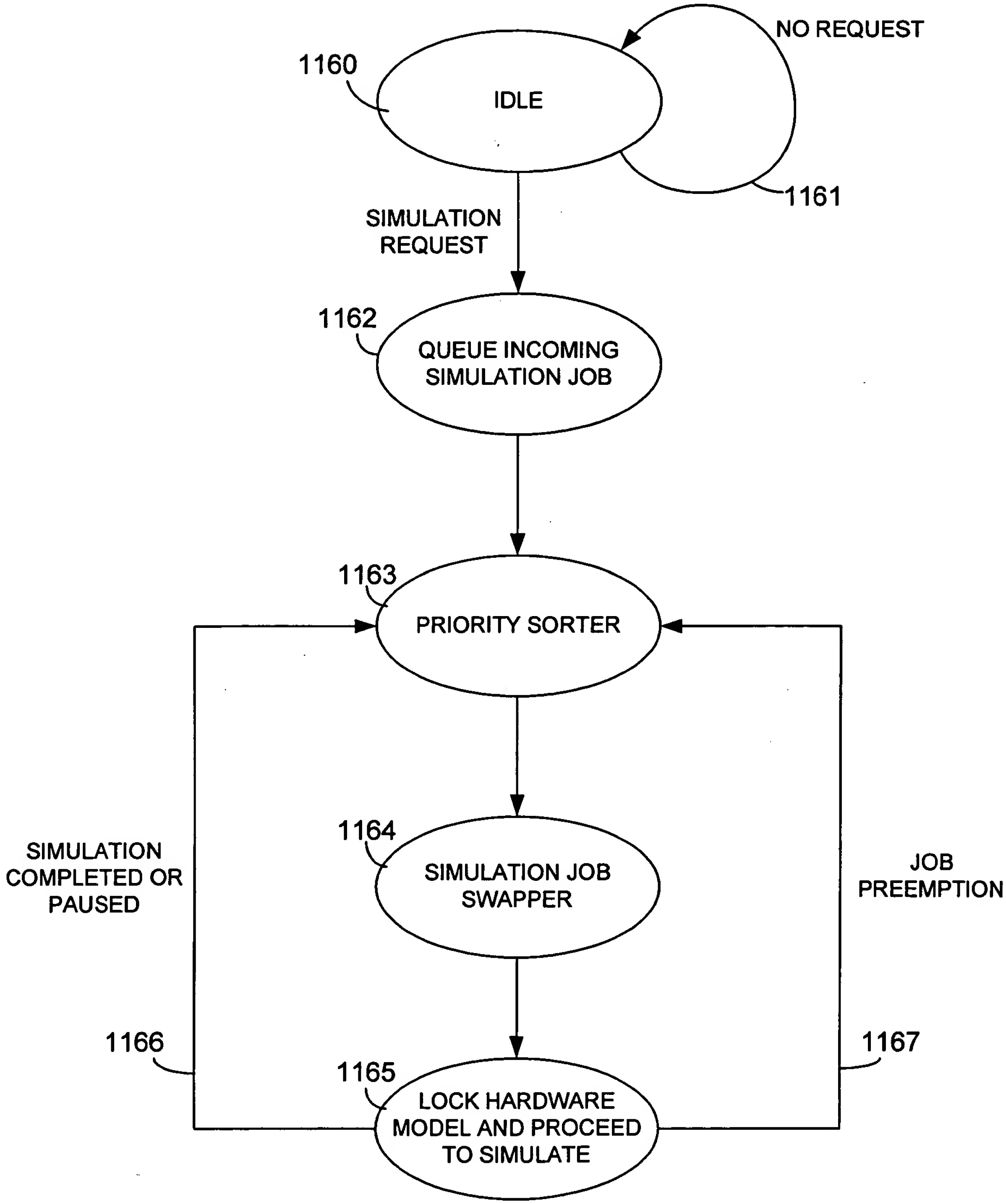


FIG. 48



NO REQUEST
1160
IDLE
1161
SIMULATION REQUEST
1162
QUEUE INCOMING SIMULATION JOB
1163
PRIORITY SORTER
1164
SIMULATION JOB SWAPPER
SIMULATION COMPLETED OR PAUSED
JOB PREEMPTION
1166
1167
1165
LOCK HARDWARE MODEL AND PROCEED TO SIMULATE

FIG. 49

JOB SWAPPER

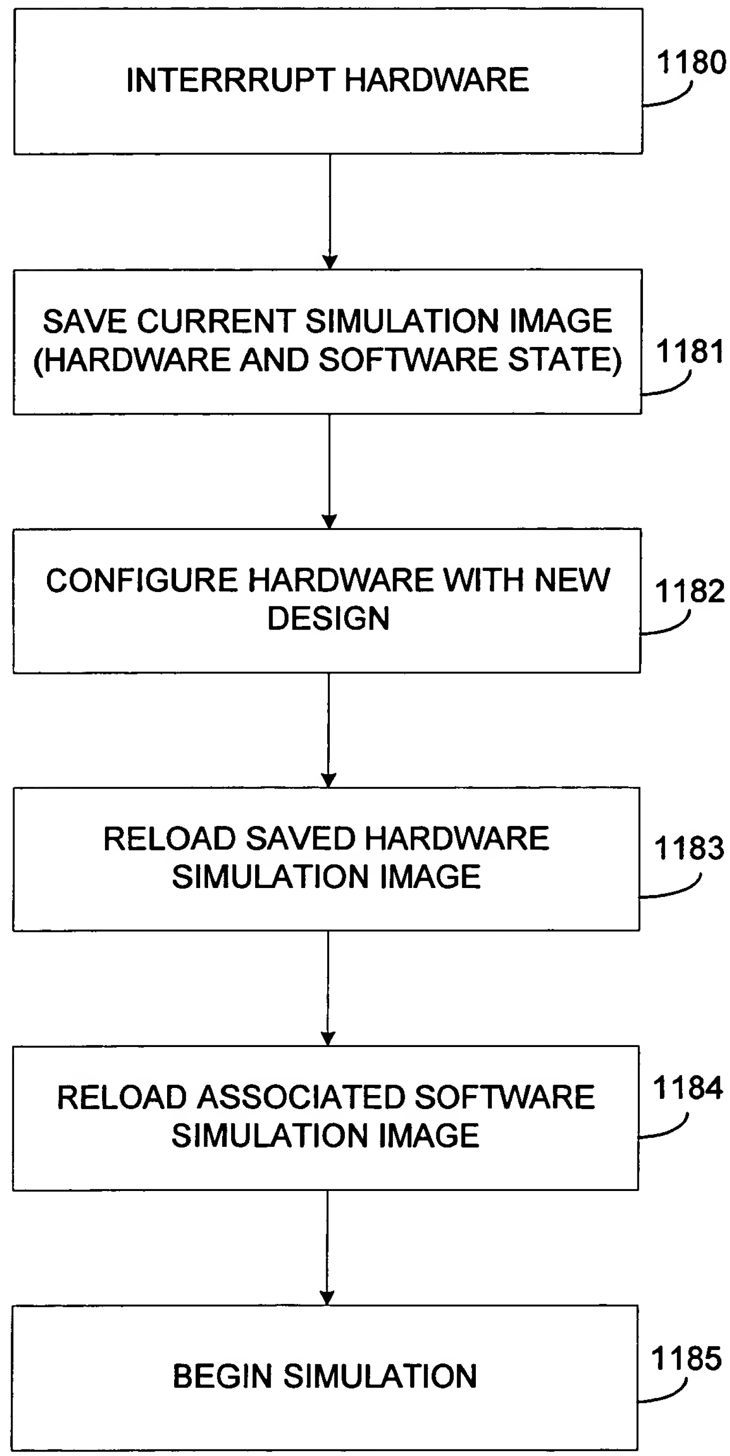


FIG. 50

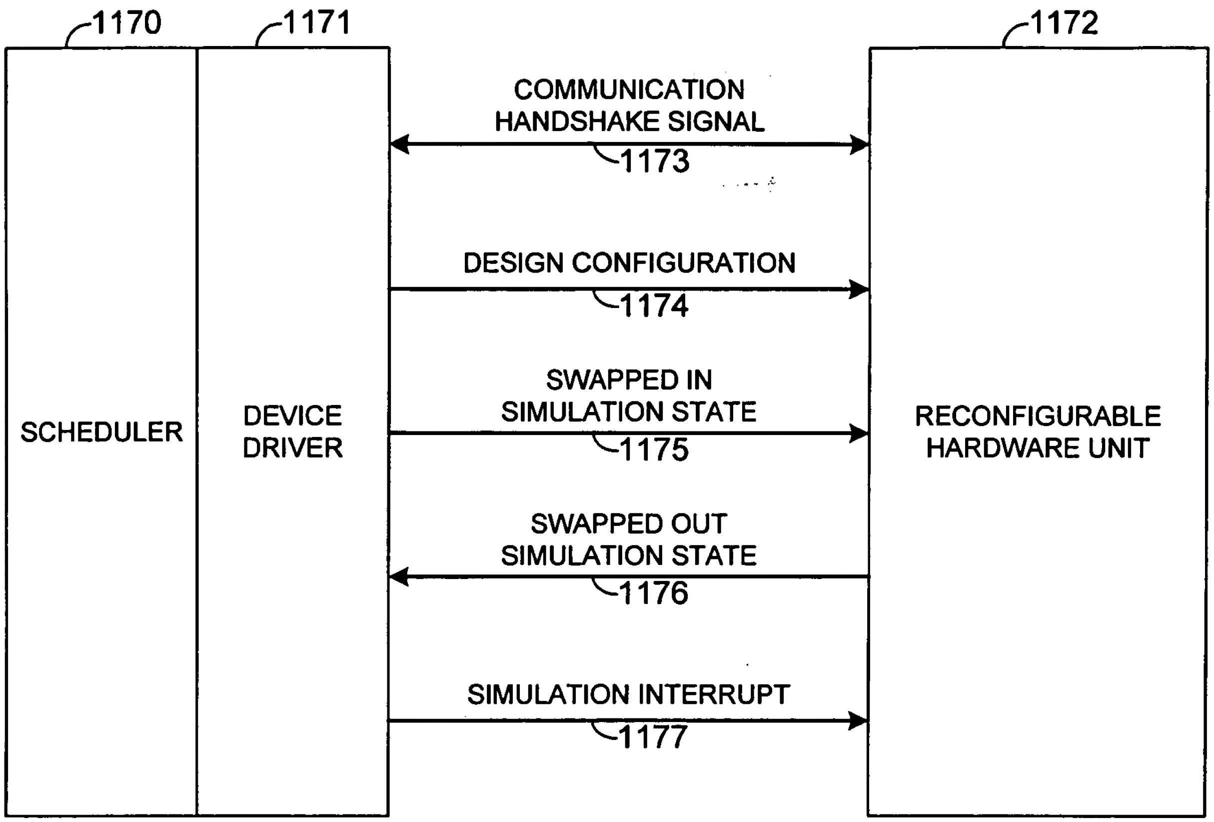

1170
1171
1172
SCHEDULER
DEVICE DRIVER
RECONFIGURABLE HARDWARE UNIT
COMMUNICATION HANDSHAKE SIGNAL
1173
DESIGN CONFIGURATION
1174
SWAPPED IN SIMULATION STATE
1175
SWAPPED OUT SIMULATION STATE
1176
SIMULATION INTERRUPT
1177

FIG. 51

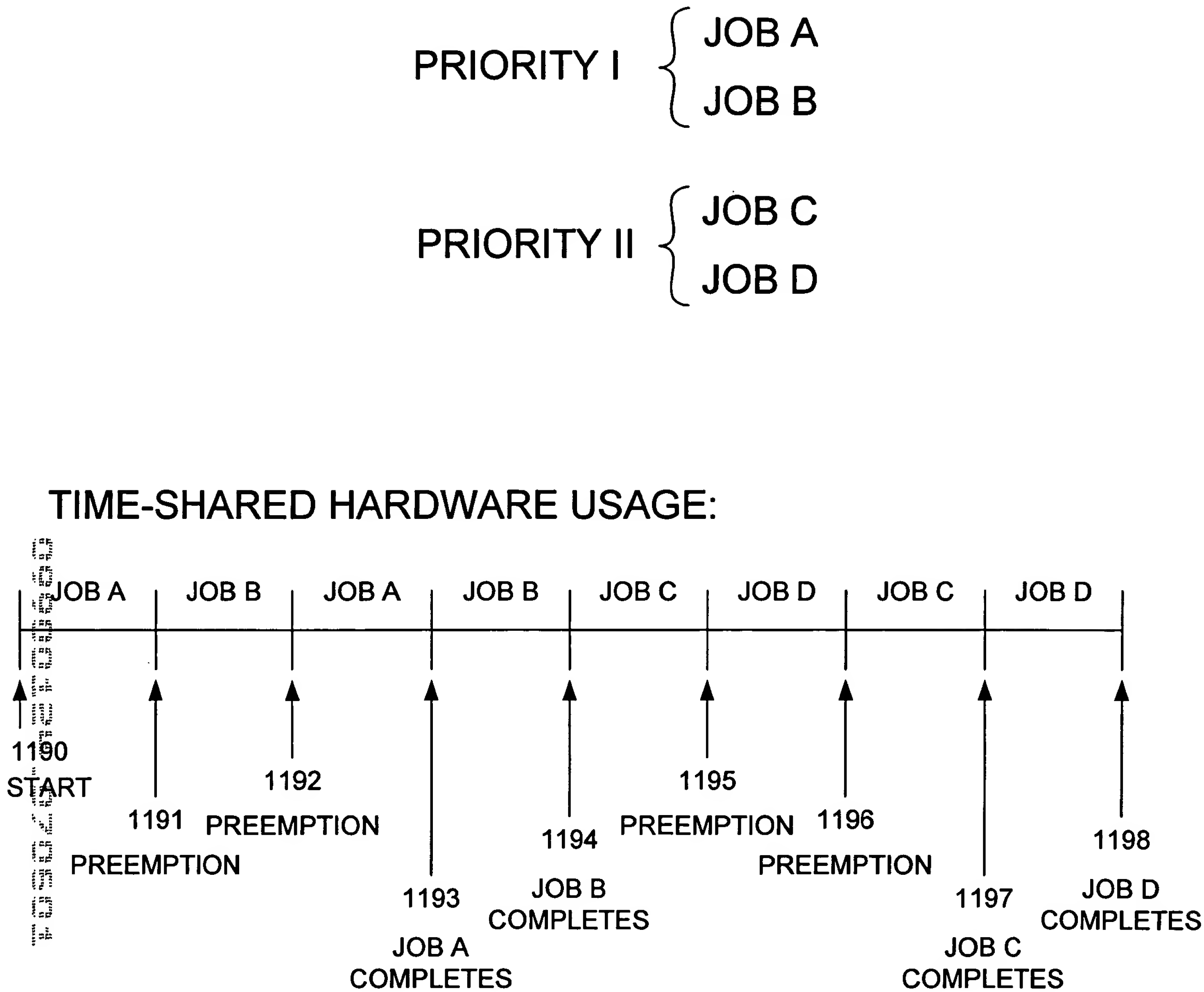

PRIORITY I
JOB A
JOB B
PRIORITY II
JOB C
JOB D
TIME-SHARED HARDWARE USAGE:
JOB A
JOB B
JOB A
JOB B
JOB C
JOB D
JOB C
JOB D
1190
START
1191
PREEMPTION
1192
PREEMPTION
1193
JOB A
COMPLETES
1194
JOB B
COMPLETES
1195
PREEMPTION
1196
PREEMPTION
1197
JOB C
COMPLETES
1198
JOB D
COMPLETES

FIG. 52

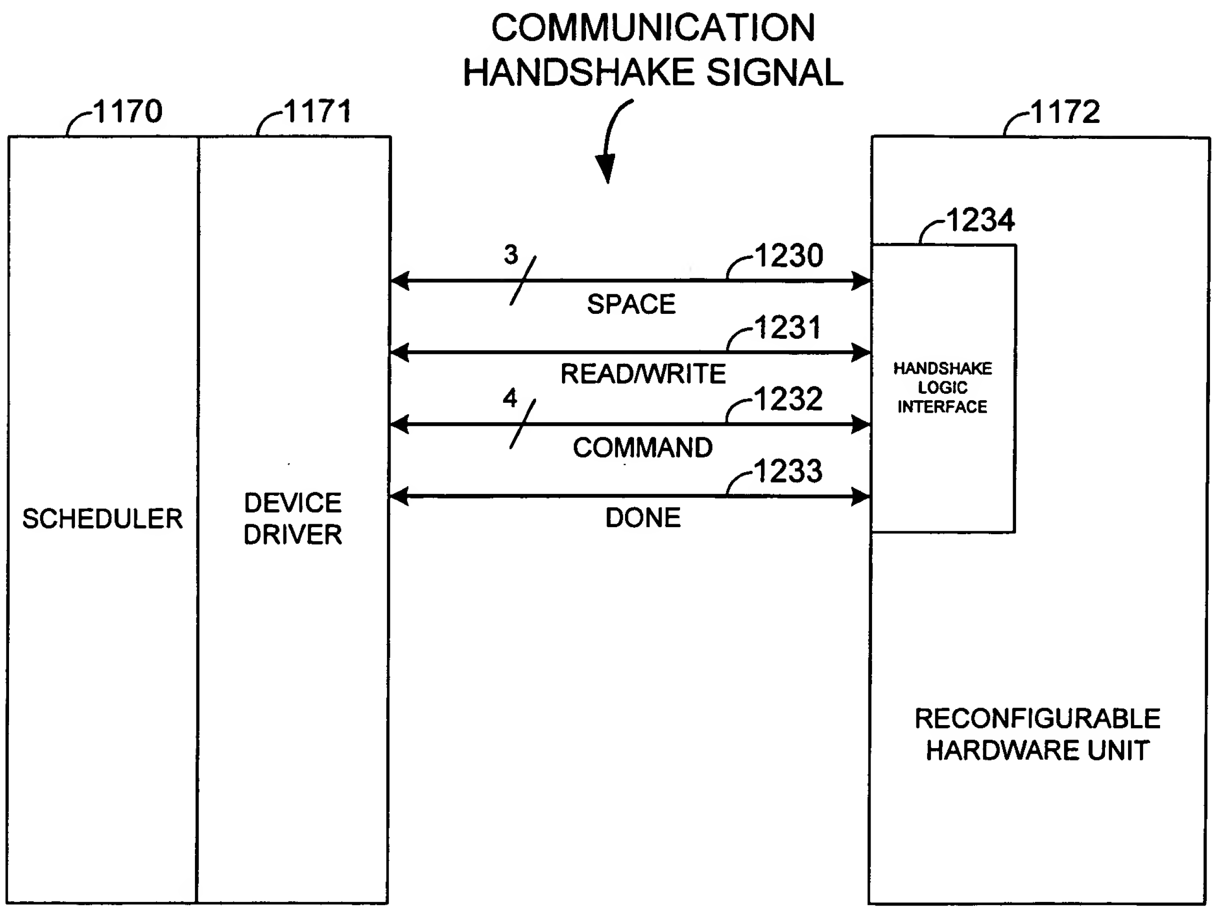

COMMUNICATION
HANDSHAKE SIGNAL
1170
1171
1172
1234
3
1230
SPACE
1231
READ/WRITE
4
1232
COMMAND
1233
DONE
HANDSHAKE
LOGIC
INTERFACE
SCHEDULER
DEVICE
DRIVER
RECONFIGURABLE
HARDWARE UNIT

FIG. 53

COMMUNICATION HANDSHAKE PROTOCOL

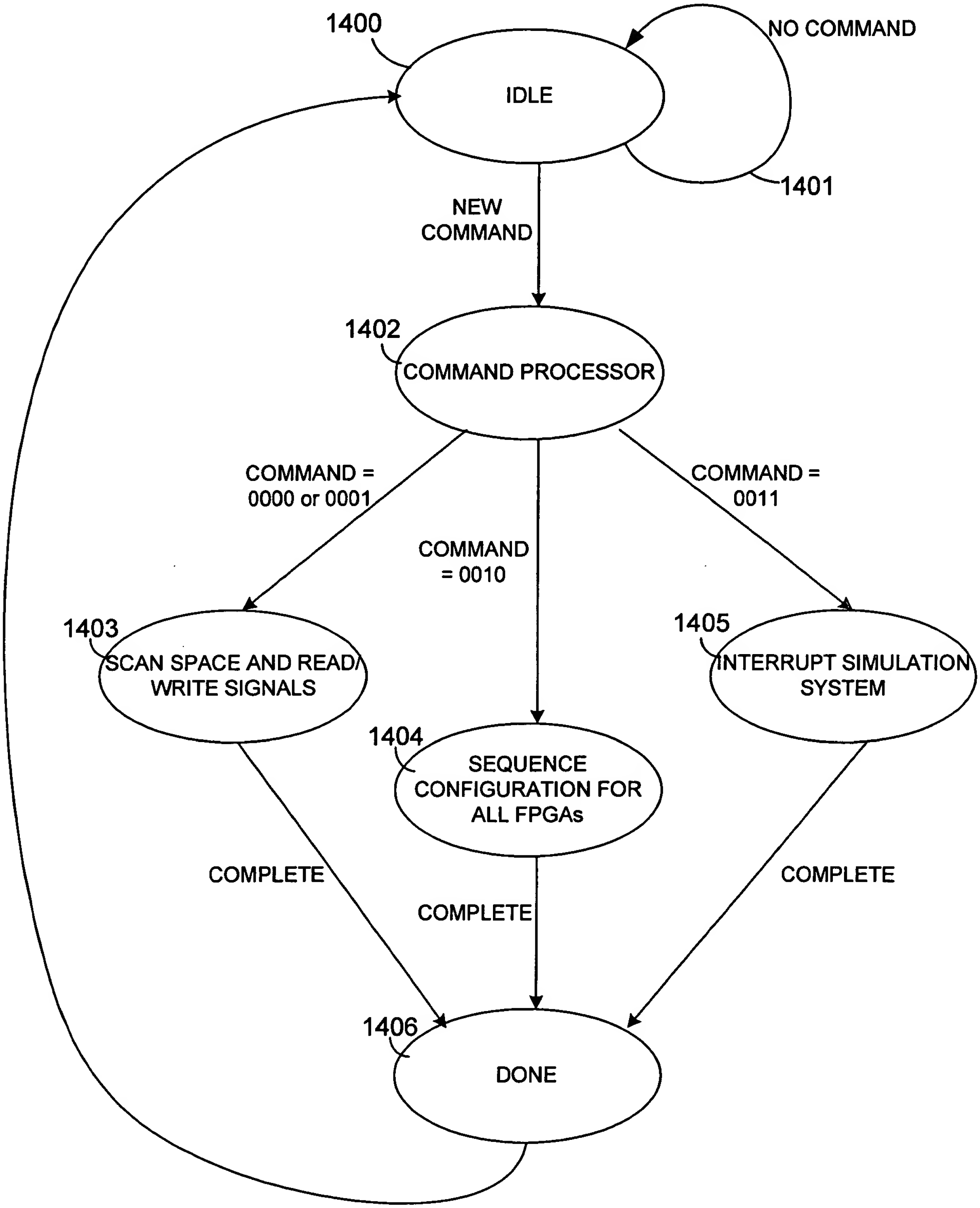
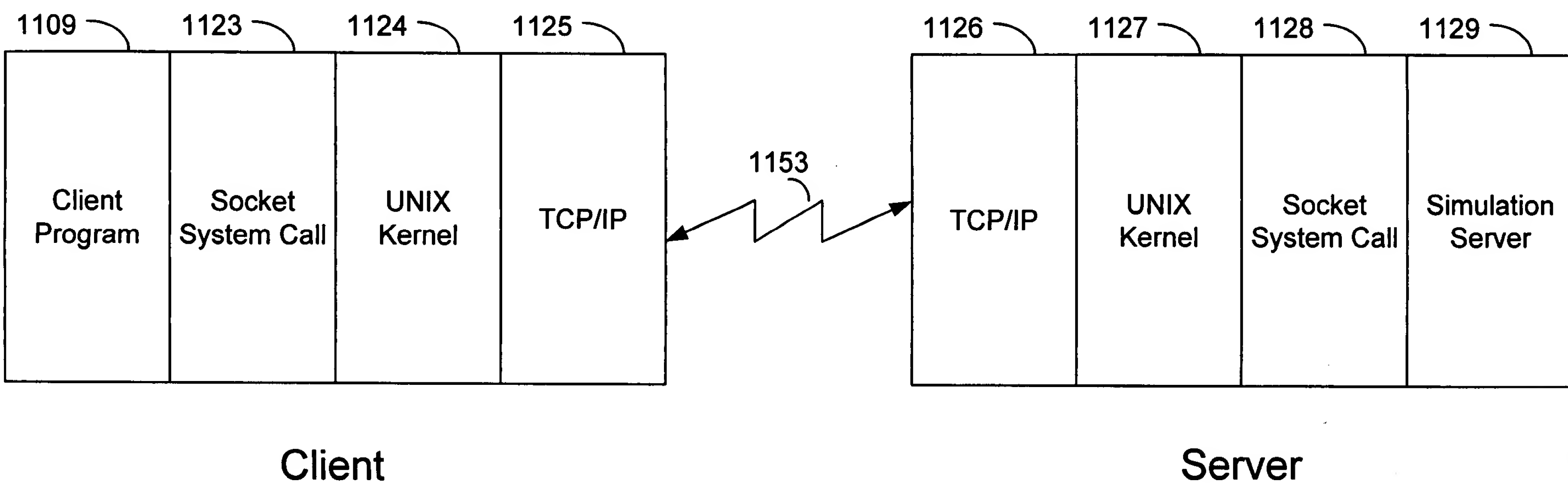


FIG. 54



1109
1123
1124
1125
Client Program
Socket System Call
UNIX Kernel
TCP/IP
1153
1126
1127
1128
1129
TCP/IP
UNIX Kernel
Socket System Call
Simulation Server
Client
Server

FIG. 55

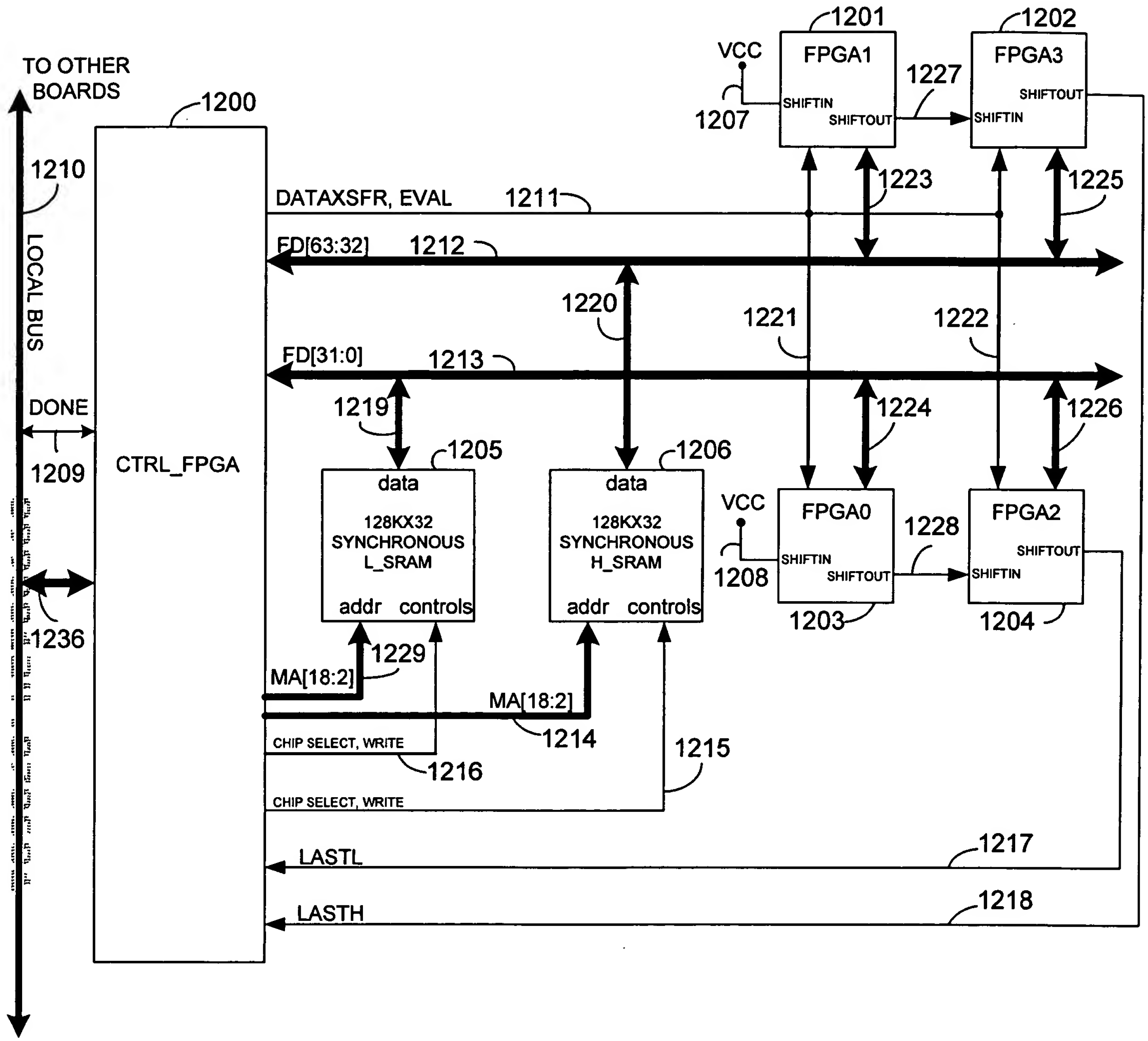

TO OTHER BOARDS
1200
1210
LOCAL BUS
DONE
1209
CTRL_FPGA
1236
VCC
1207
FPGA1
SHIFTIN
SHIFTOUT
1201
1227
FPGA3
SHIFTOUT
SHIFTIN
1202
1223
1225
DATAXSFR, EVAL
1211
FD[63:32]
1212
1220
1221
1222
FD[31:0]
1213
1219
1224
1226
1205
data
128KX32
SYNCHRONOUS
L_SRAM
addr
controls
1206
data
128KX32
SYNCHRONOUS
H_SRAM
addr
controls
VCC
1208
FPGA0
SHIFTIN
SHIFTOUT
1203
1228
FPGA2
SHIFTOUT
SHIFTIN
1204
1229
MA[18:2]
MA[18:2]
1214
CHIP SELECT, WRITE
1216
1215
CHIP SELECT, WRITE
LASTL
1217
LASTH
1218

FIG. 56

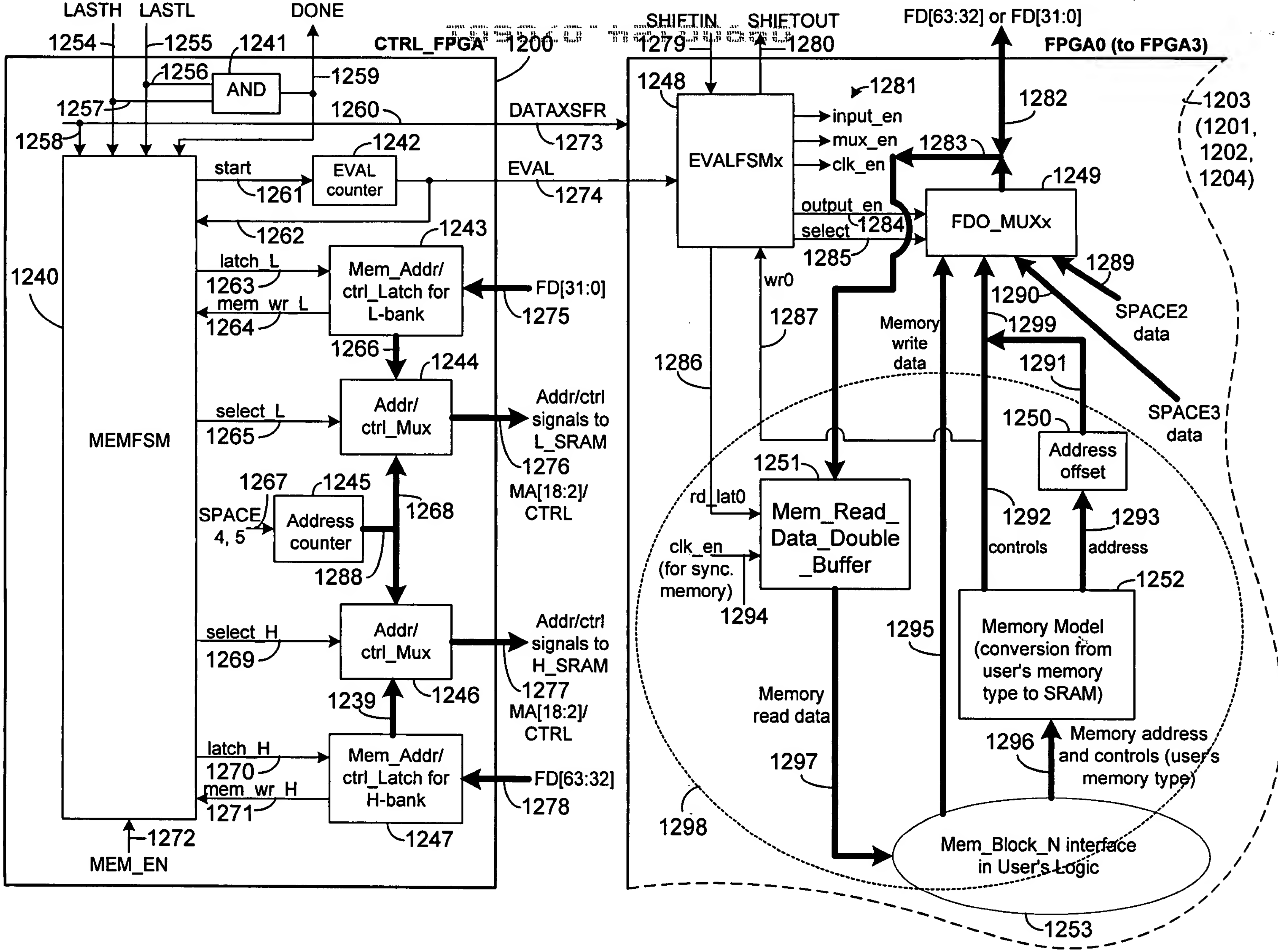

LASTH
LASTL
DONE
CTRL_FPGA
1200
AND
MEMFSM
start
EVAL counter
latch_L
mem_wr_L
Mem_Addr/ ctrl_Latch for L-bank
FD[31:0]
select_L
Addr/ ctrl_Mux
Addr/ctrl signals to L_SRAM
MA[18:2]/ CTRL
SPACE 4, 5
Address counter
select_H
Addr/ctrl signals to H_SRAM
latch_H
mem_wr_H
Mem_Addr/ ctrl_Latch for H-bank
FD[63:32]
MEM_EN
DATAXSFR
EVAL
SHIFTIN
SHIFTOUT
FD[63:32] or FD[31:0]
FPGA0 (to FPGA3)
EVALFSMx
input_en
mux_en
clk_en
output_en
select
FDO_MUXx
wr0
SPACE2 data
SPACE3 data
Memory write data
Address offset
rd_lat0
Mem_Read_ Data_Double _Buffer
clk_en (for sync. memory)
controls
address
Memory Model (conversion from user's memory type to SRAM)
Memory read data
Memory address and controls (user's memory type)
Mem_Block_N interface in User's Logic
1203 (1201, 1202, 1204)

FIG. 57

MEMFSM - Memory Finite State Machine in CTRL_FPGA unit

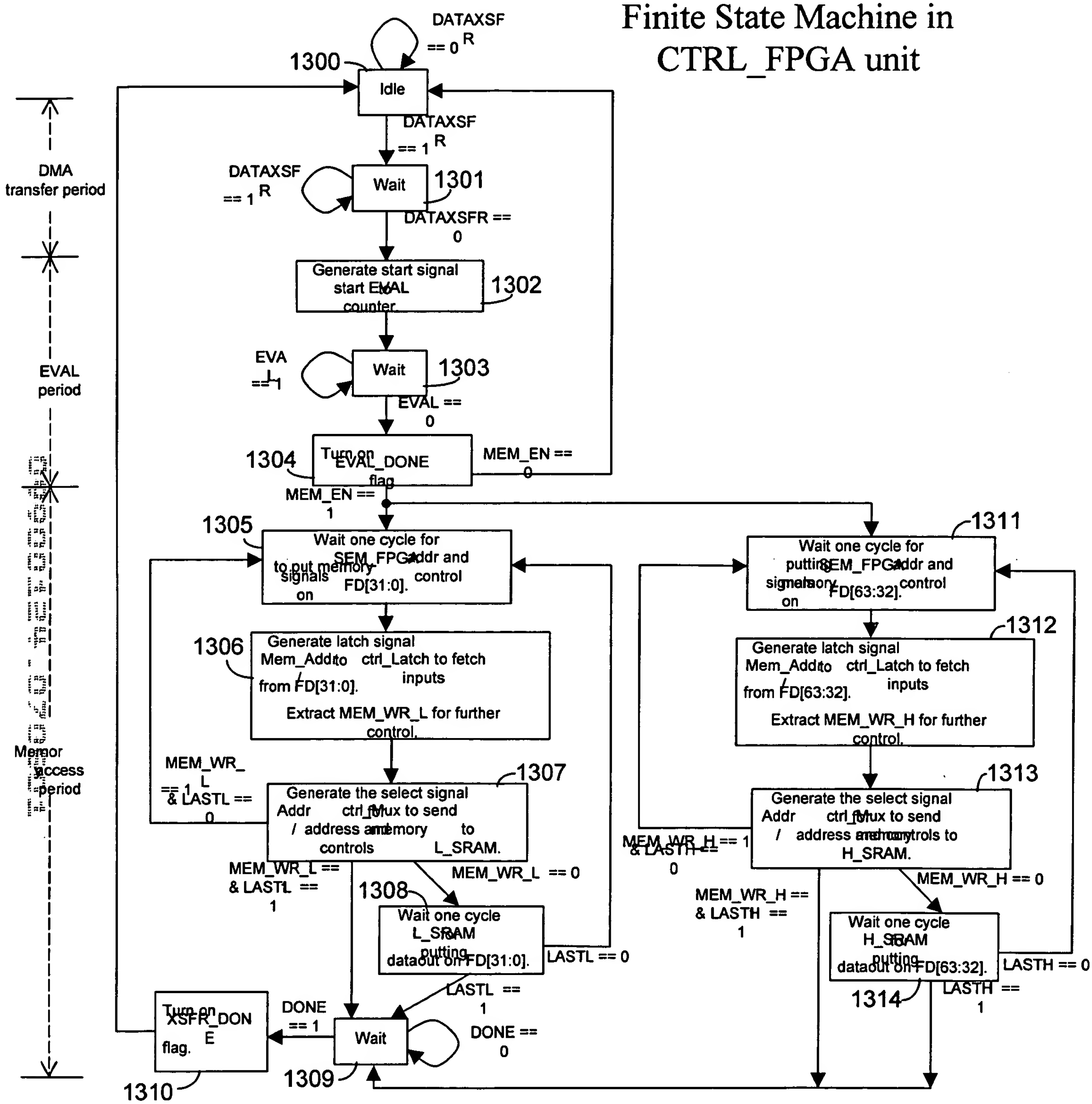


FIG. 58

EVALFSM - EVAL Finite State Machine in each FPGA logic device

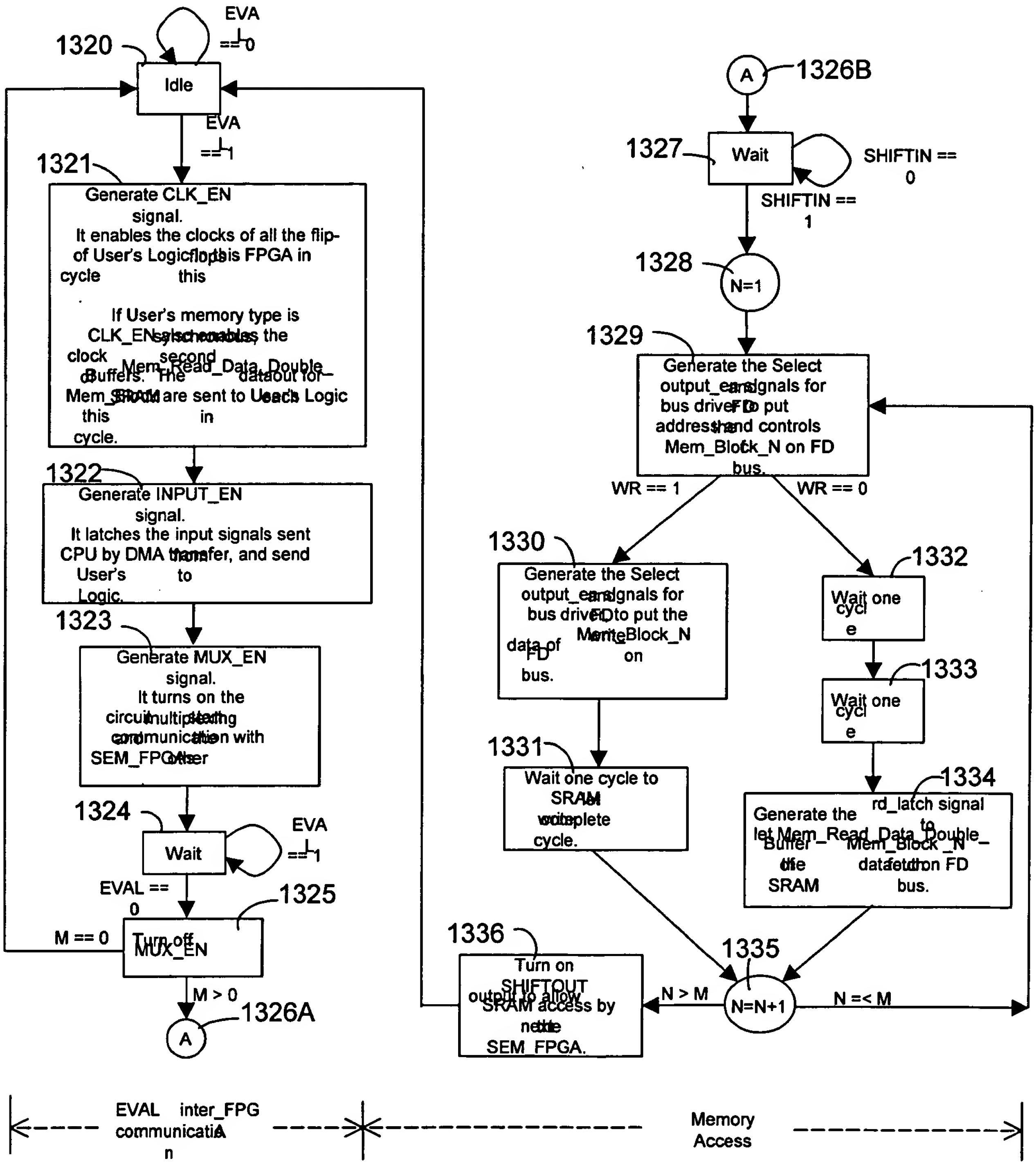


FIG. 59

MEMORY READ DATA
DOUBLE BUFFER

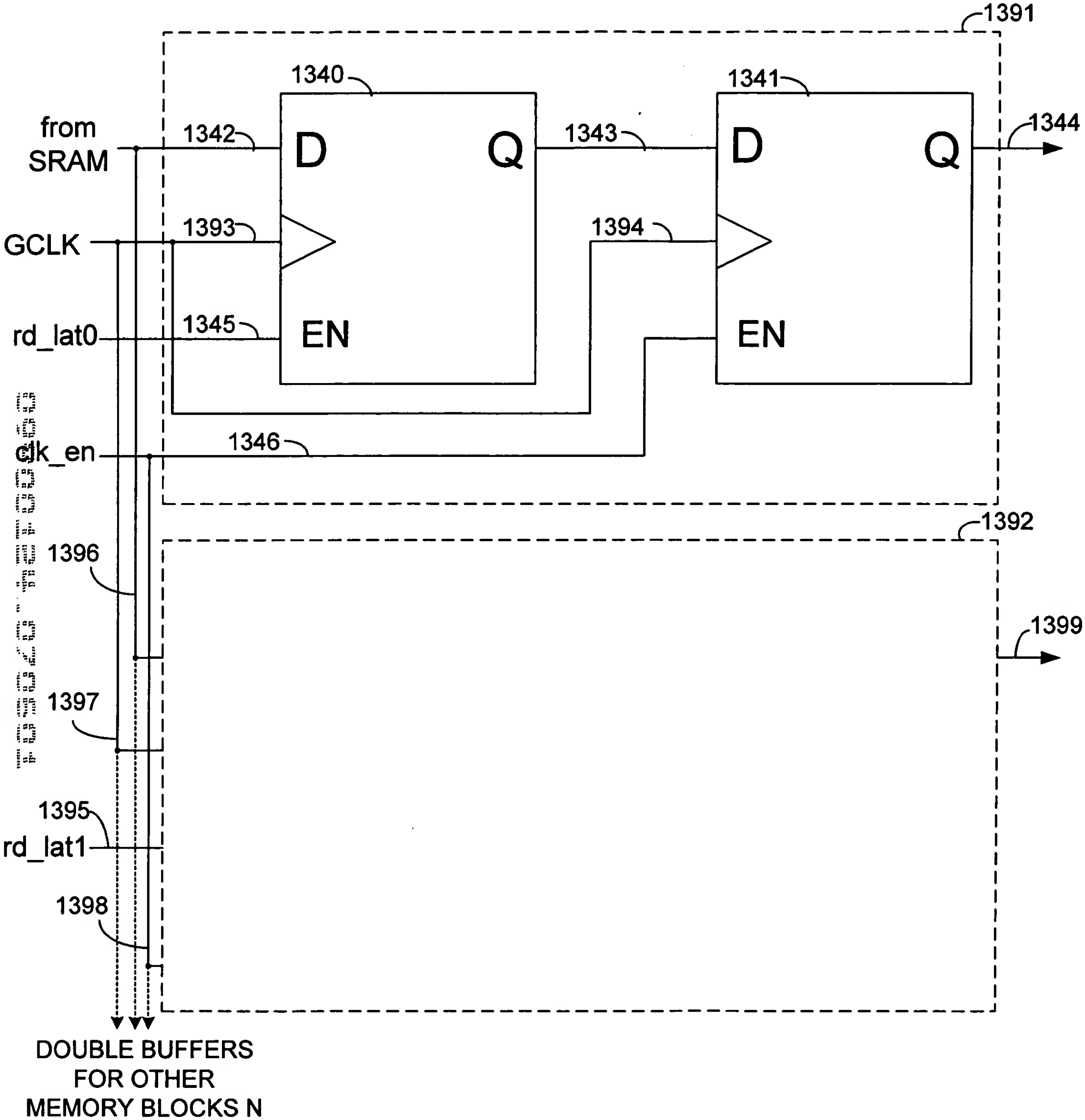


FIG. 60

SIMULATION WRITE/READ CYCLE

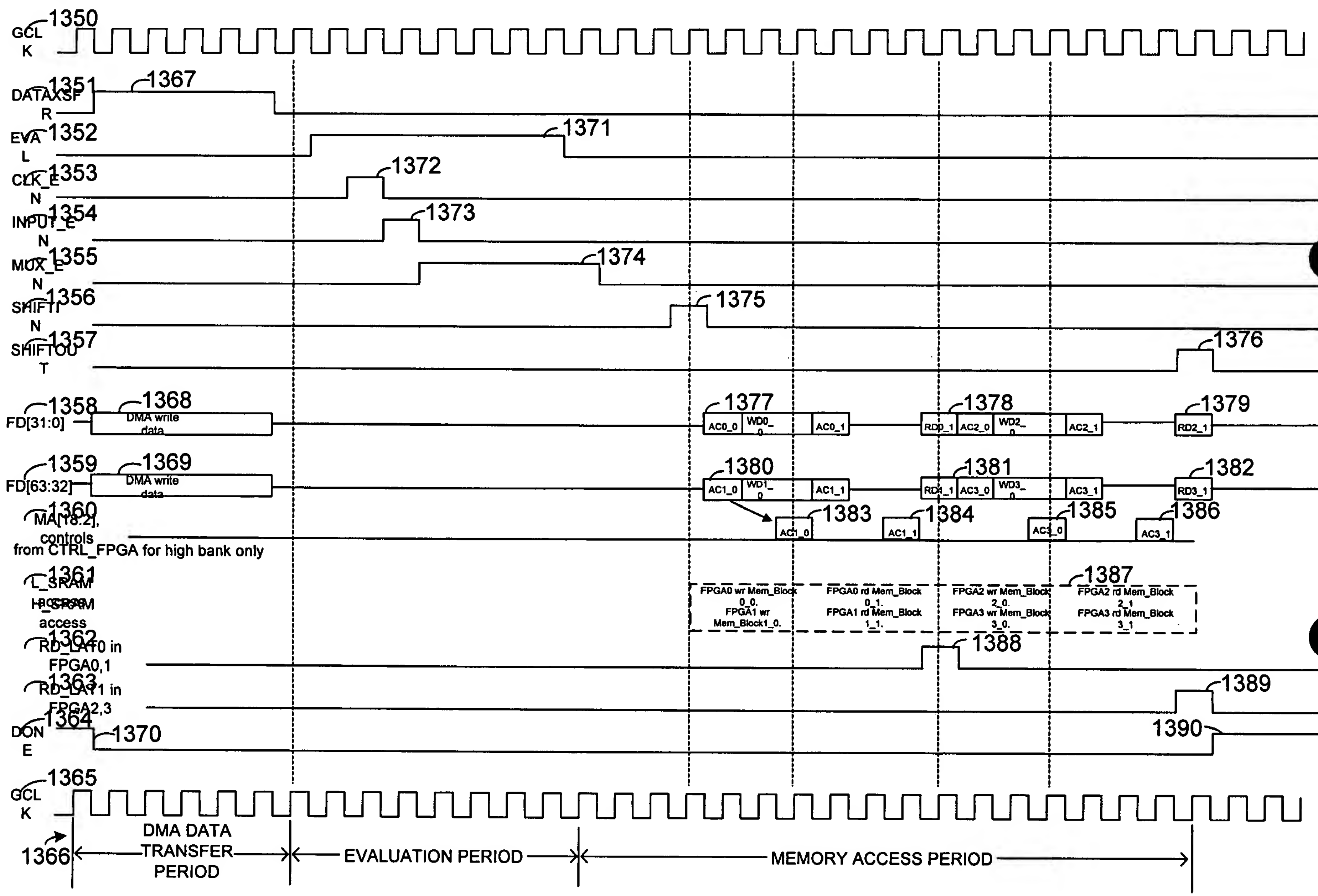
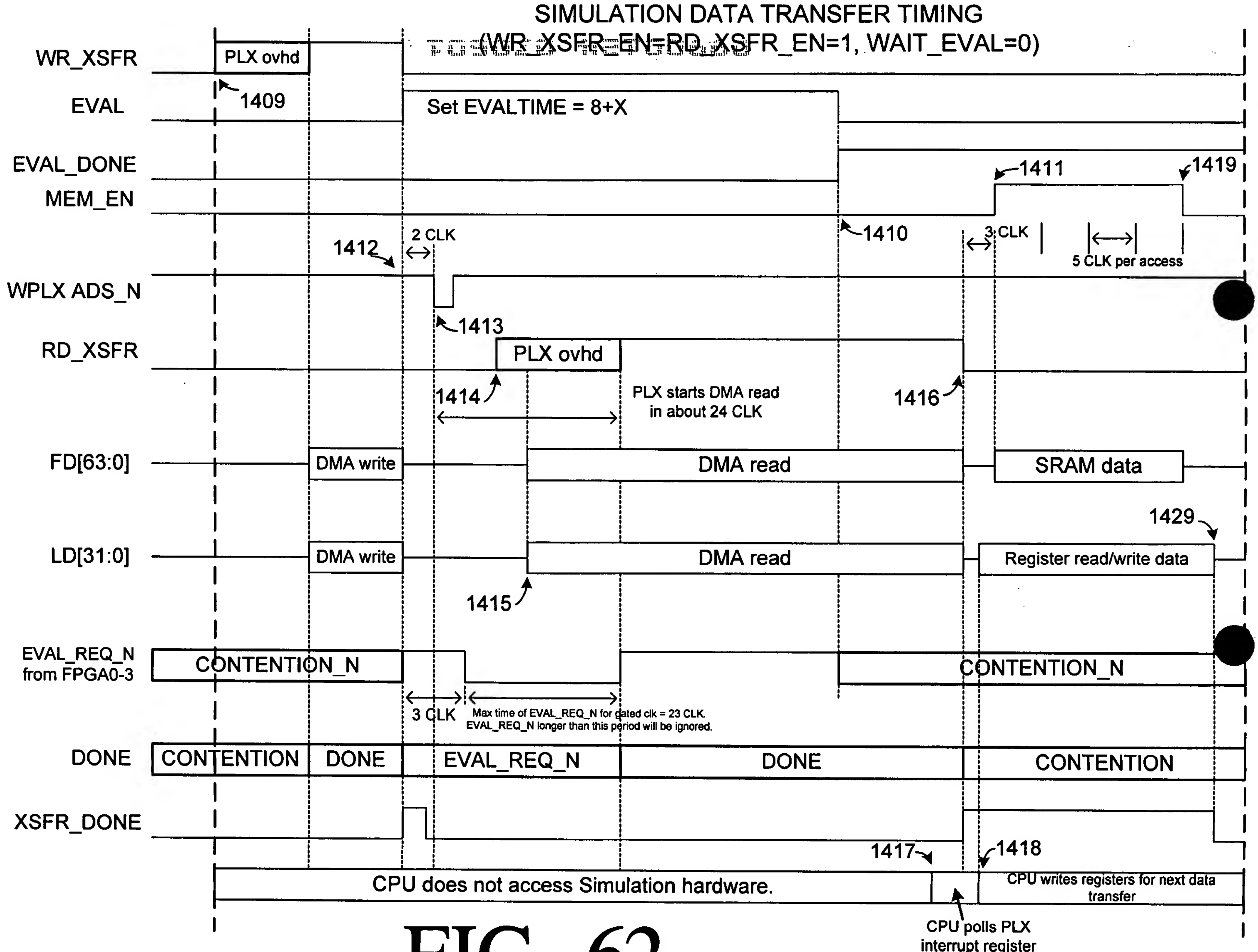


FIG. 61



SIMULATION DATA TRANSFER TIMING
(WR_XSFR_EN=RD_XSFR_EN=1, WAIT_EVAL=0)
WR_XSFR
EVAL
EVAL_DONE
MEM_EN
WPLX ADS_N
RD_XSFR
FD[63:0]
LD[31:0]
EVAL_REQ_N from FPGA0-3
DONE
XSFR_DONE
PLX ovhd
1409
Set EVALTIME = 8+X
1411
1419
1410
1412
2 CLK
3 CLK
5 CLK per access
1413
PLX ovhd
1414
PLX starts DMA read in about 24 CLK
1416
DMA write
DMA read
SRAM data
1429
DMA write
DMA read
Register read/write data
1415
CONTENTION_N
CONTENTION_N
3 CLK
Max time of EVAL_REQ_N for gated clk = 23 CLK.
EVAL_REQ_N longer than this period will be ignored.
CONTENTION
DONE
EVAL_REQ_N
DONE
CONTENTION
1417
1418
CPU does not access Simulation hardware.
CPU writes registers for next data transfer
CPU polls PLX interrupt register

FIG. 62

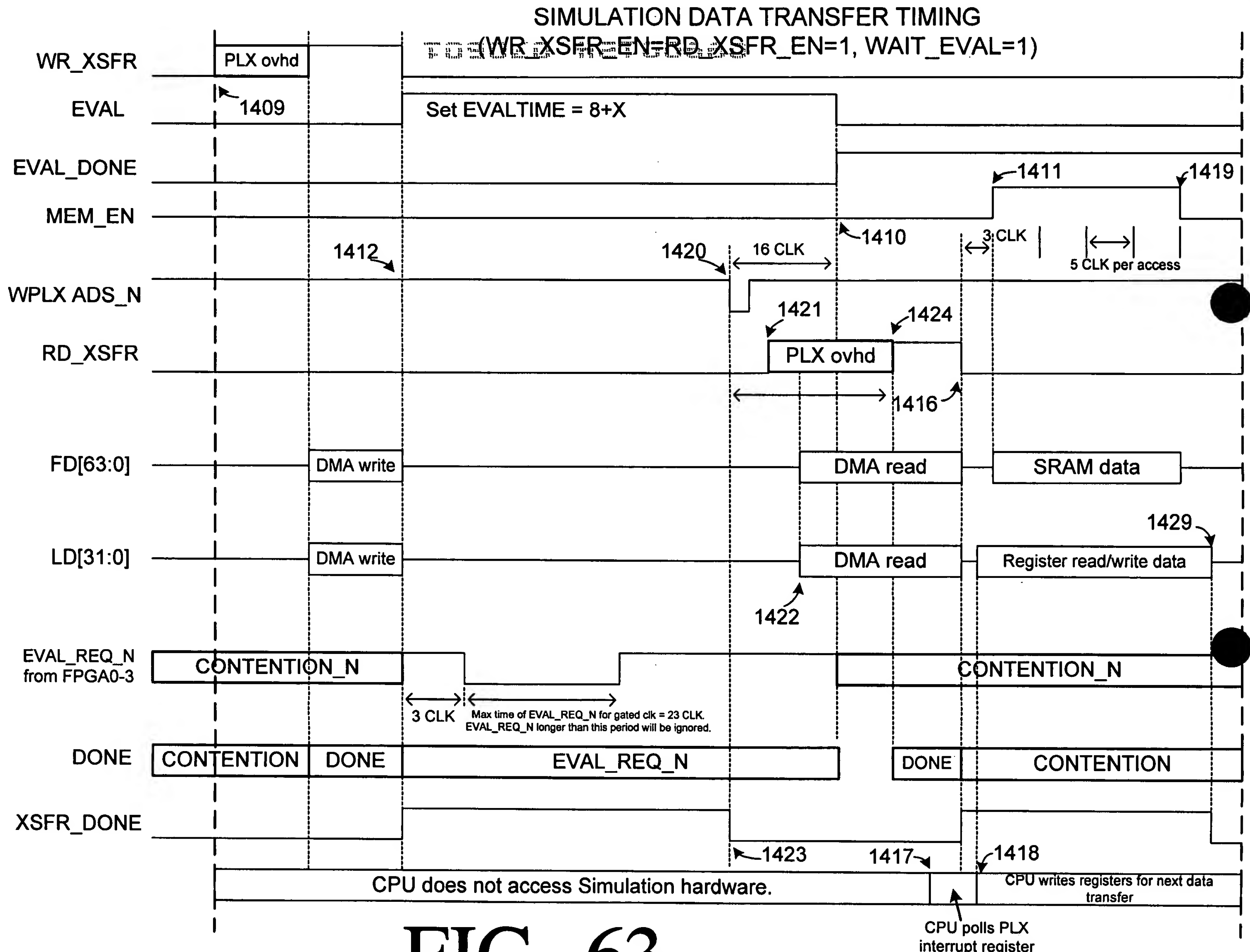

SIMULATION DATA TRANSFER TIMING
(WR_XSFR_EN=RD_XSFR_EN=1, WAIT_EVAL=1)
WR_XSFR
EVAL
EVAL_DONE
MEM_EN
WPLX ADS_N
RD_XSFR
FD[63:0]
LD[31:0]
EVAL_REQ_N from FPGA0-3
DONE
XSFR_DONE
PLX ovhd
1409
Set EVALTIME = 8+X
1411
1419
1410
1412
1420
16 CLK
3 CLK
5 CLK per access
1421
1424
PLX ovhd
1416
DMA write
DMA read
SRAM data
1429
DMA write
DMA read
Register read/write data
1422
CONTENTION_N
CONTENTION_N
3 CLK
Max time of EVAL_REQ_N for gated clk = 23 CLK.
EVAL_REQ_N longer than this period will be ignored.
CONTENTION
DONE
EVAL_REQ_N
DONE
CONTENTION
1423
1417
1418
CPU does not access Simulation hardware.
CPU writes registers for next data transfer
CPU polls PLX interrupt register

FIG. 63

Typical User Design of PCI Add-on Cards

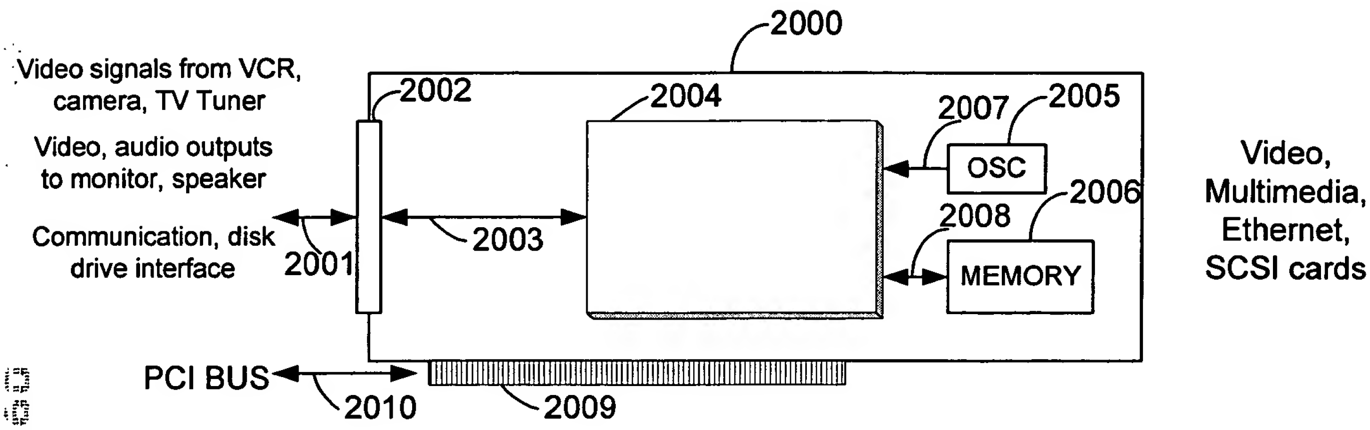


FIG. 64

Typical Hardware/Software Co-Verification

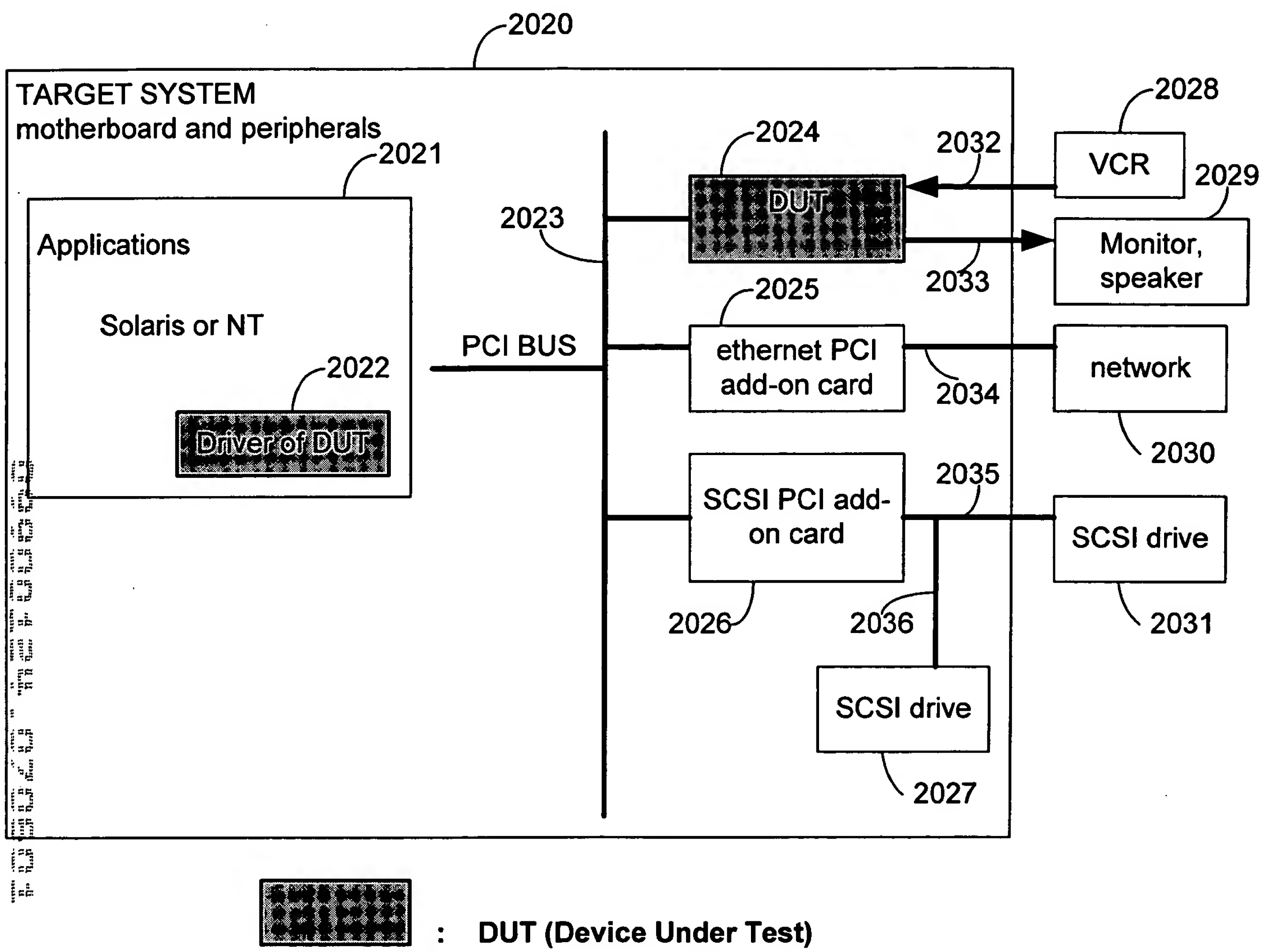


FIG. 65

Typical Co-Verification by Using Emulator

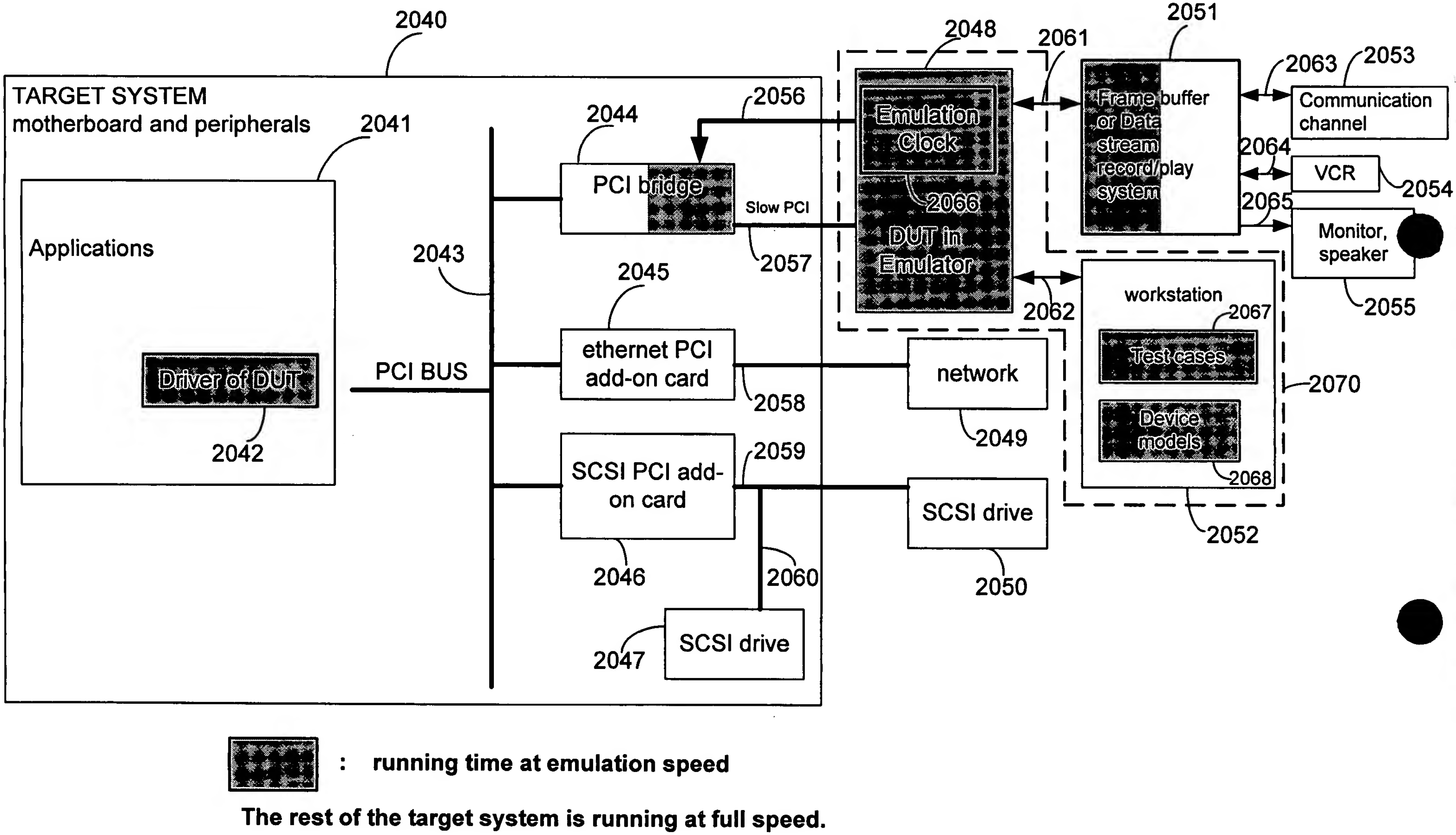


FIG. 66

SIMULATION

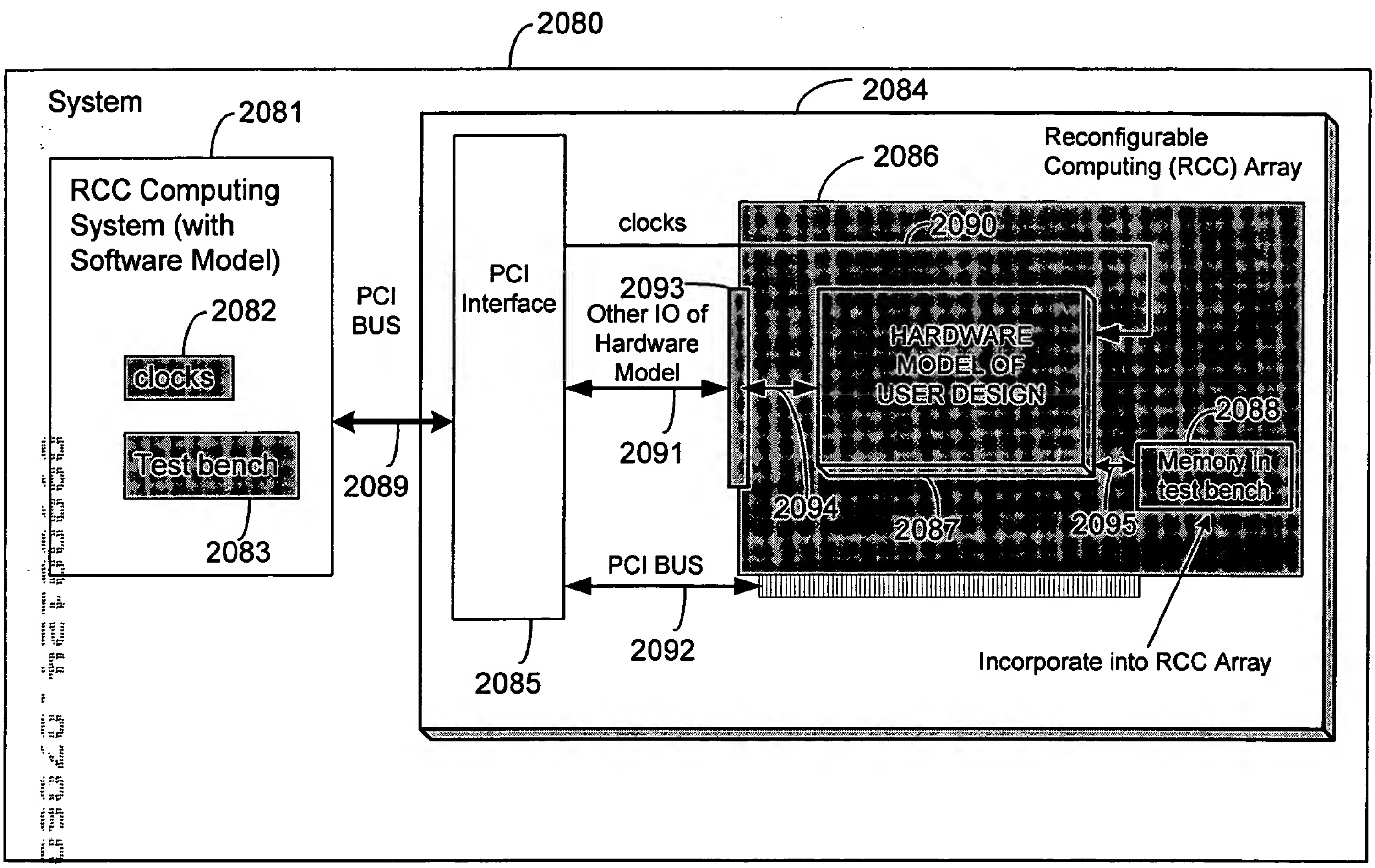


FIG. 67

CO-VERIFICATION WITHOUT EXTERNAL I/O

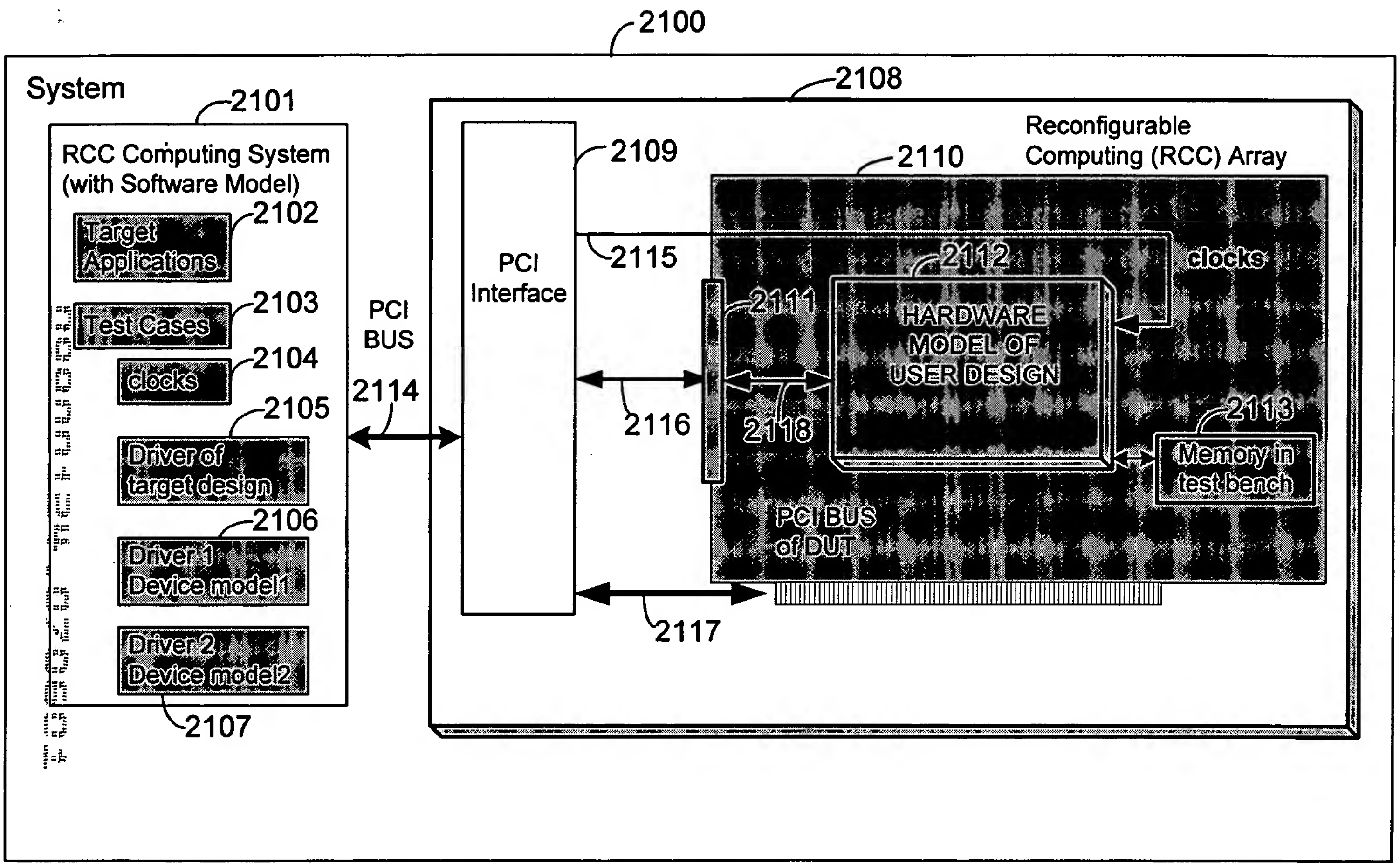


FIG. 68

CO-VERI[illegible]CATION WITH E[illegible]TERNAL I/O

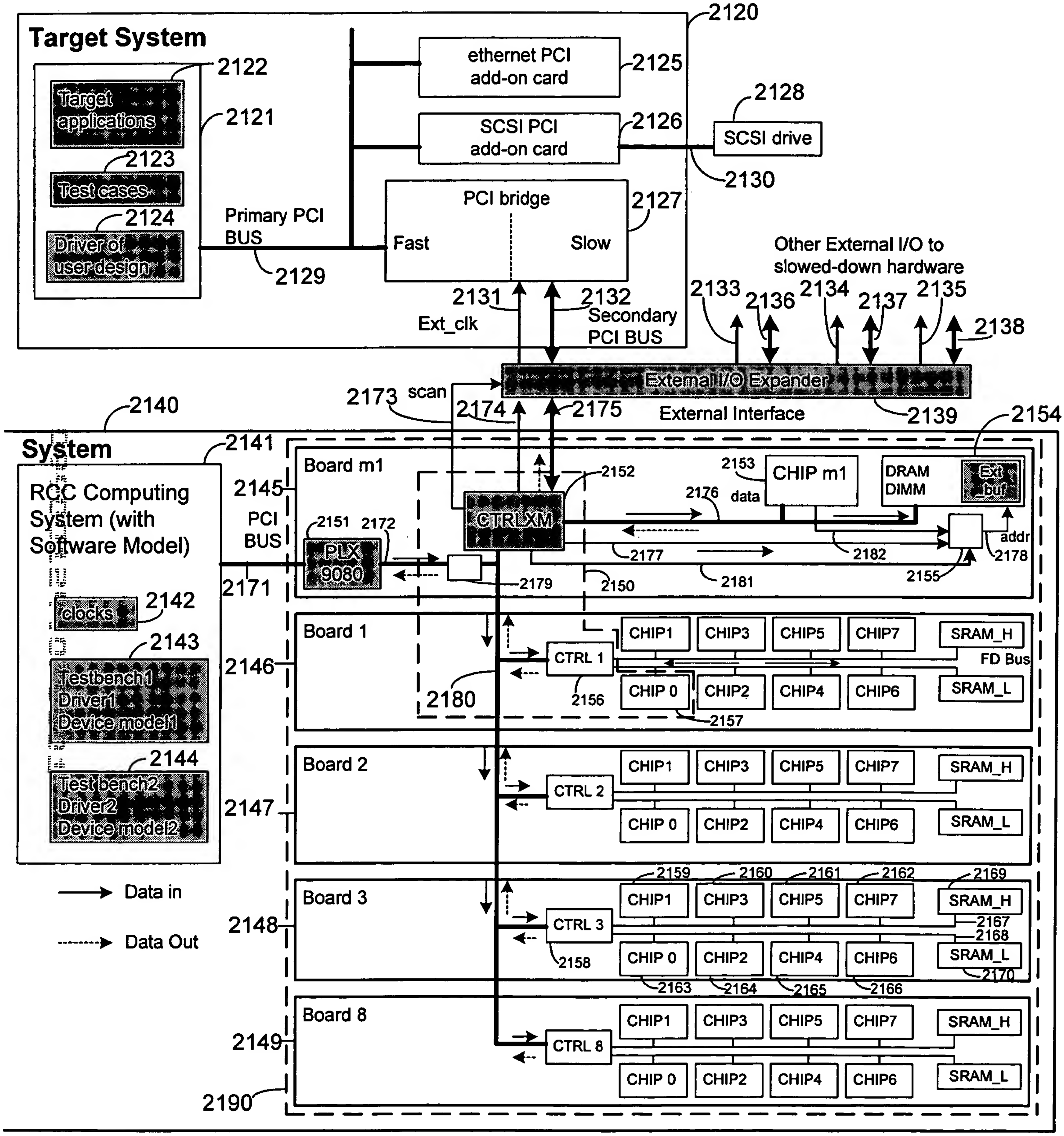


FIG. 69

CONTROL OF DATA-IN CYCLE

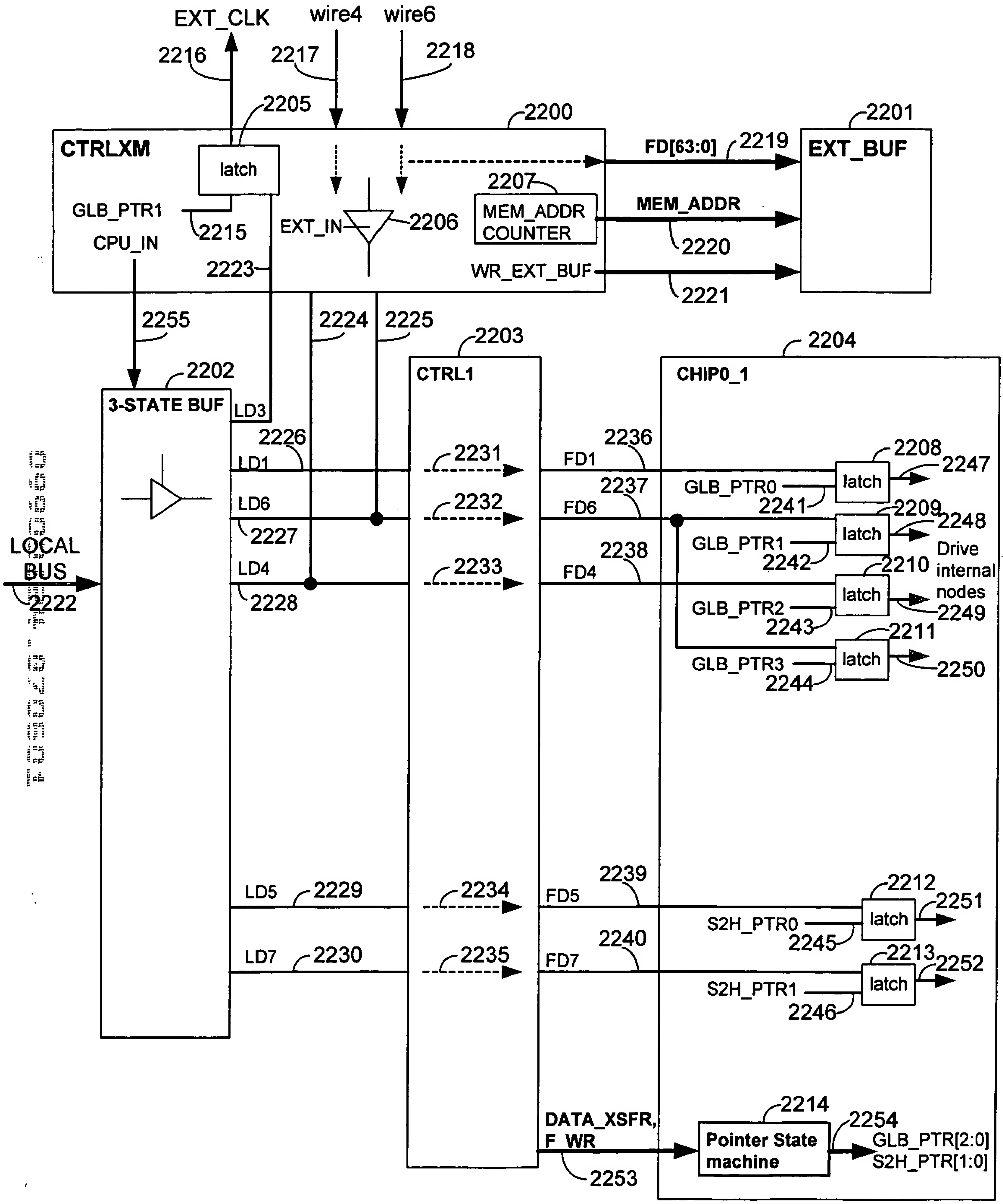


FIG. 70

CONTR●L OF DATA-OU● CYCLE

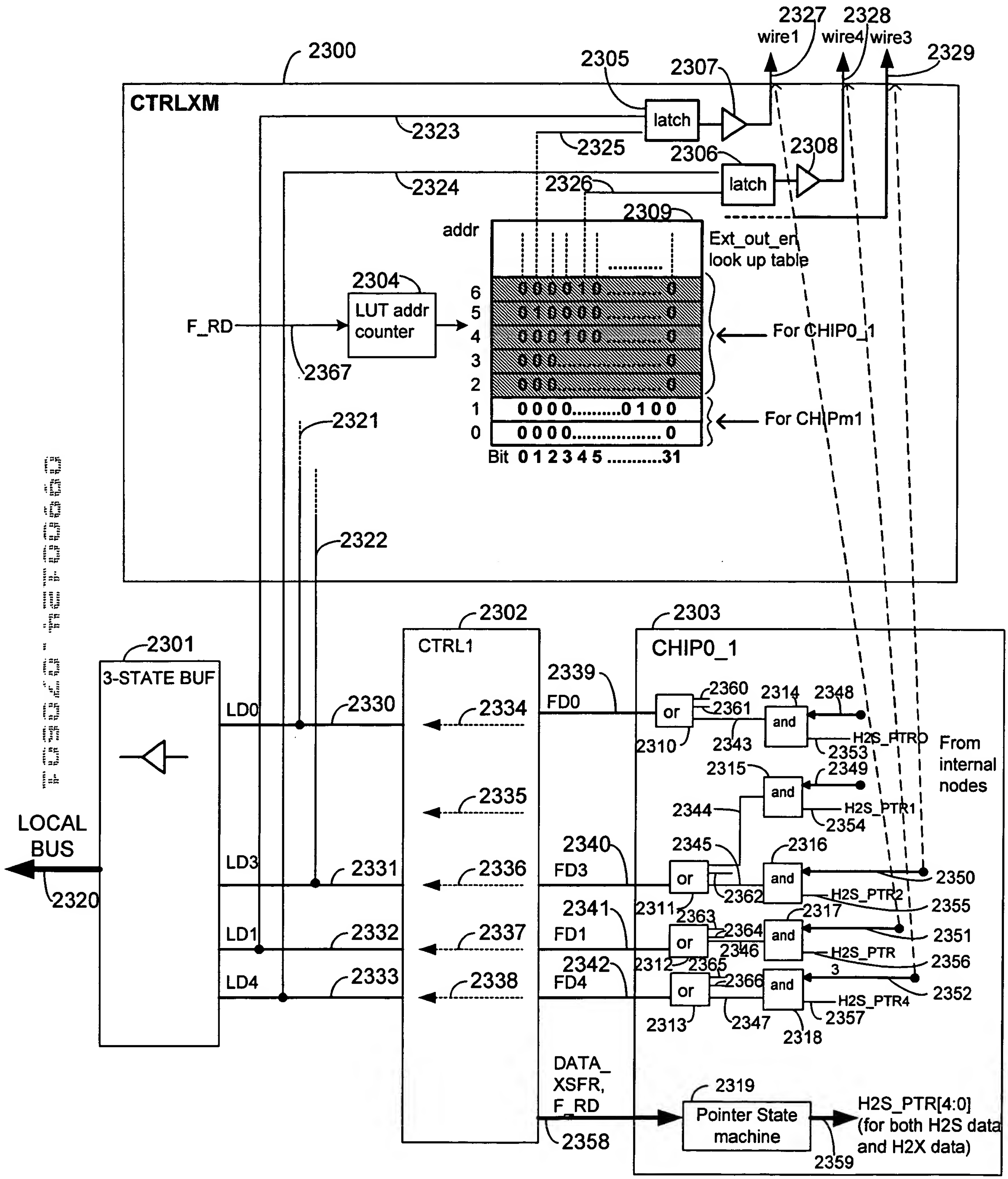


FIG. 71

CONTROL OF DATA-IN CYCLE

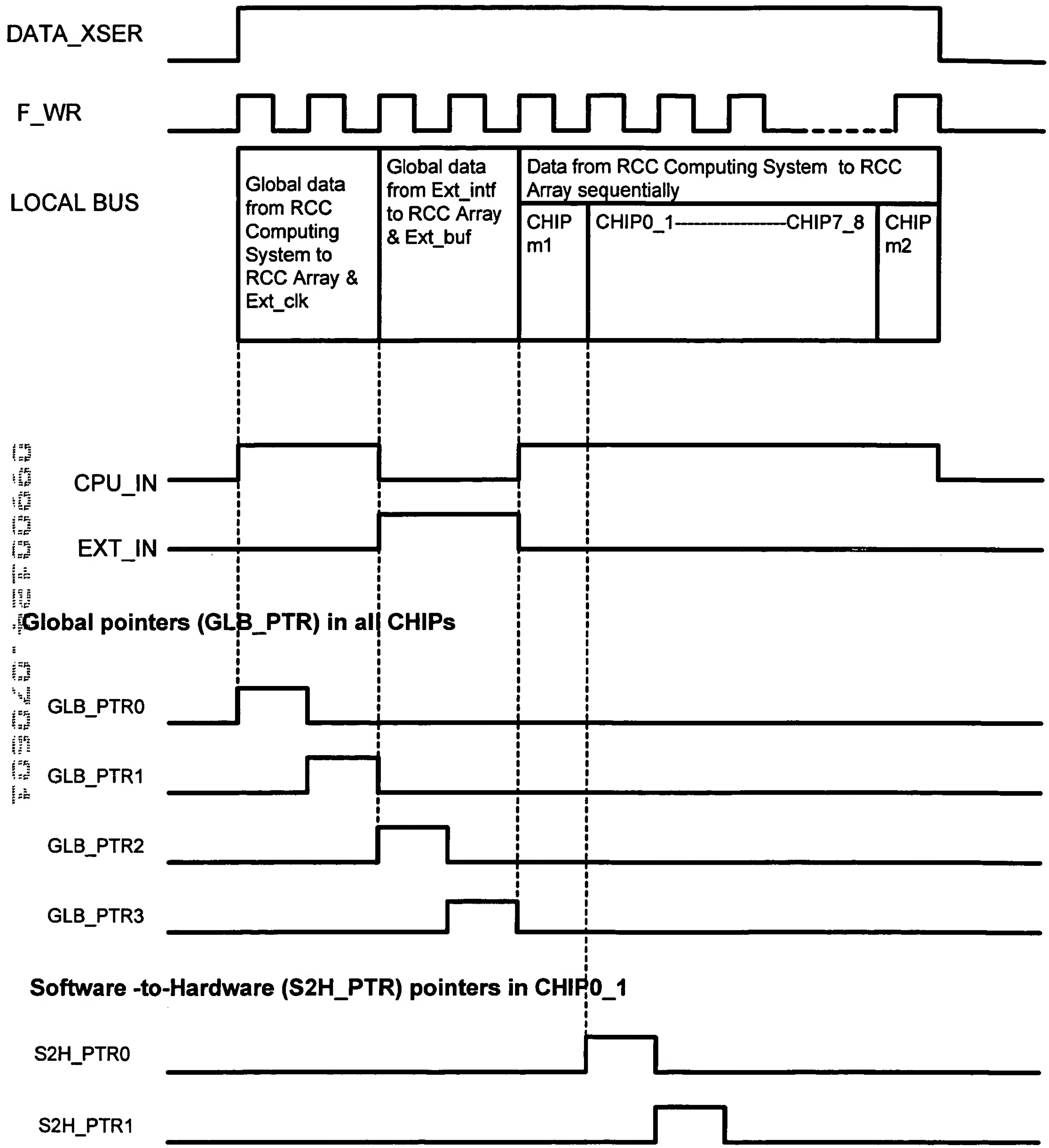


FIG. 72

CONTROL OF DATA-OUT CYCLE

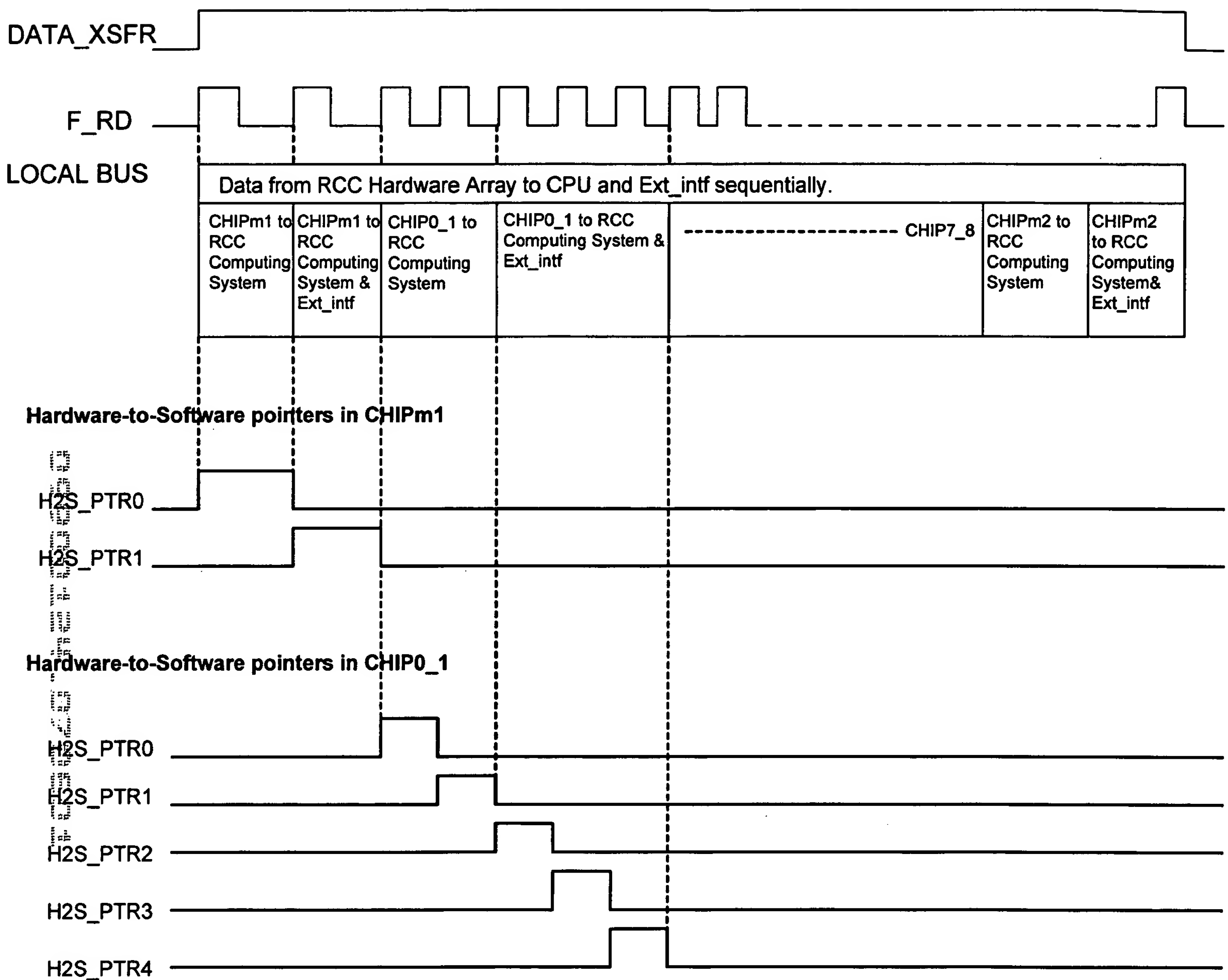
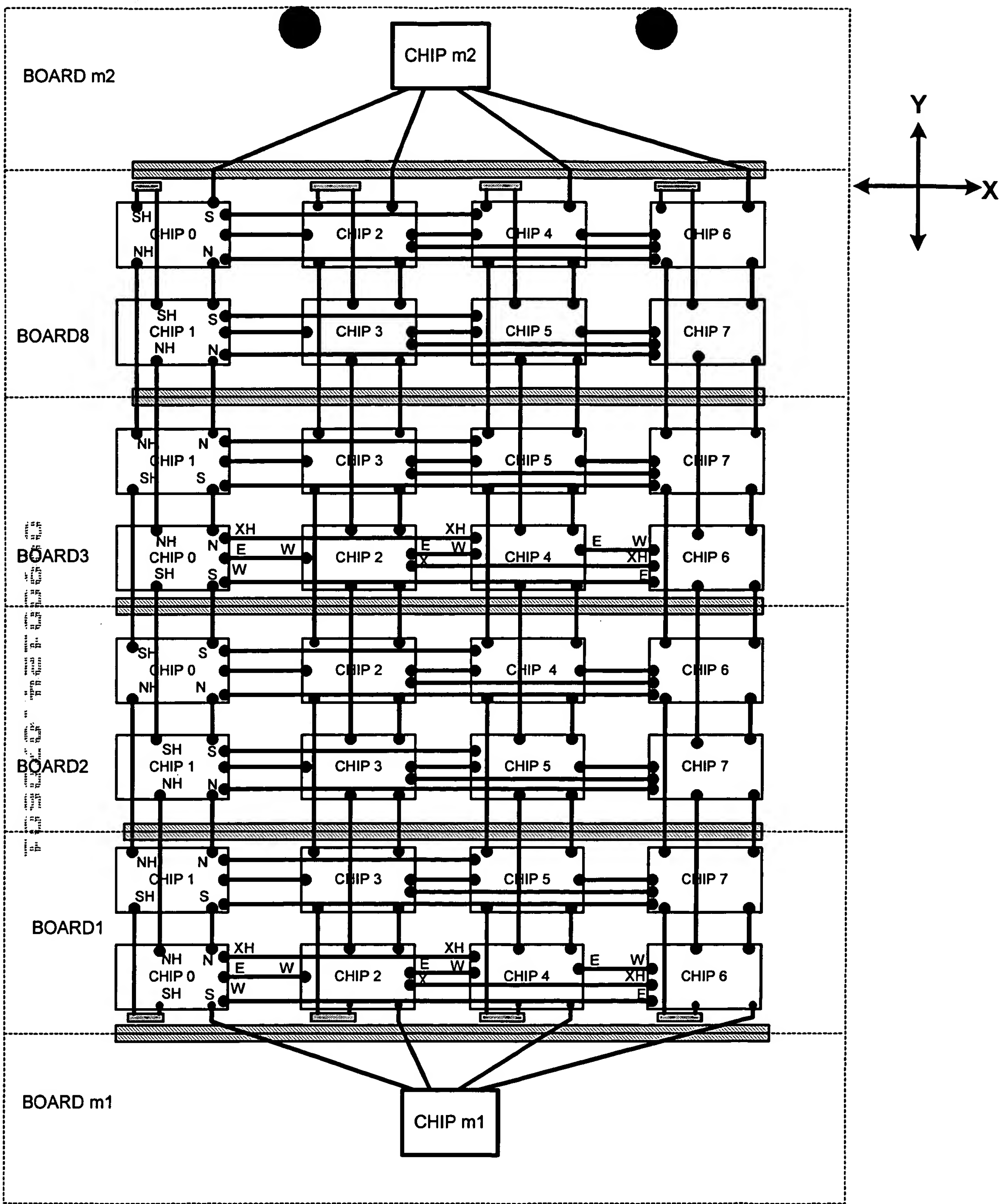


FIG. 73



BOARD m2
CHIP m2
Y
X
BOARD8
CHIP 0
SH
S
NH
N
CHIP 2
CHIP 4
CHIP 6
CHIP 1
CHIP 3
CHIP 5
CHIP 7
BOARD3
XH
E
W
BOARD2
BOARD1
BOARD m1
CHIP m1

FIG. 74

SHIFT REGISTER

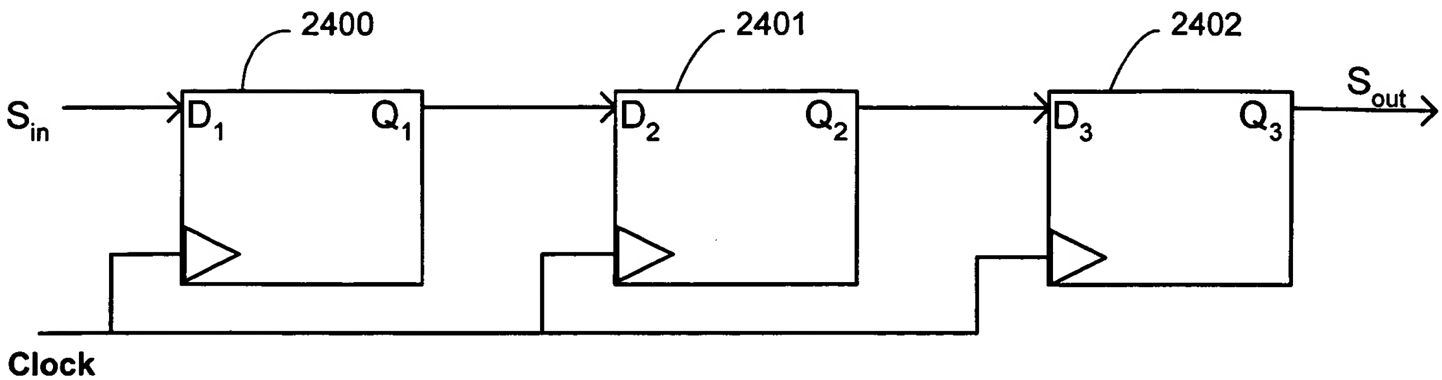


FIG. 75(A)

HOLD TIME ASSUMPTION FOR SHIFT REGISTER

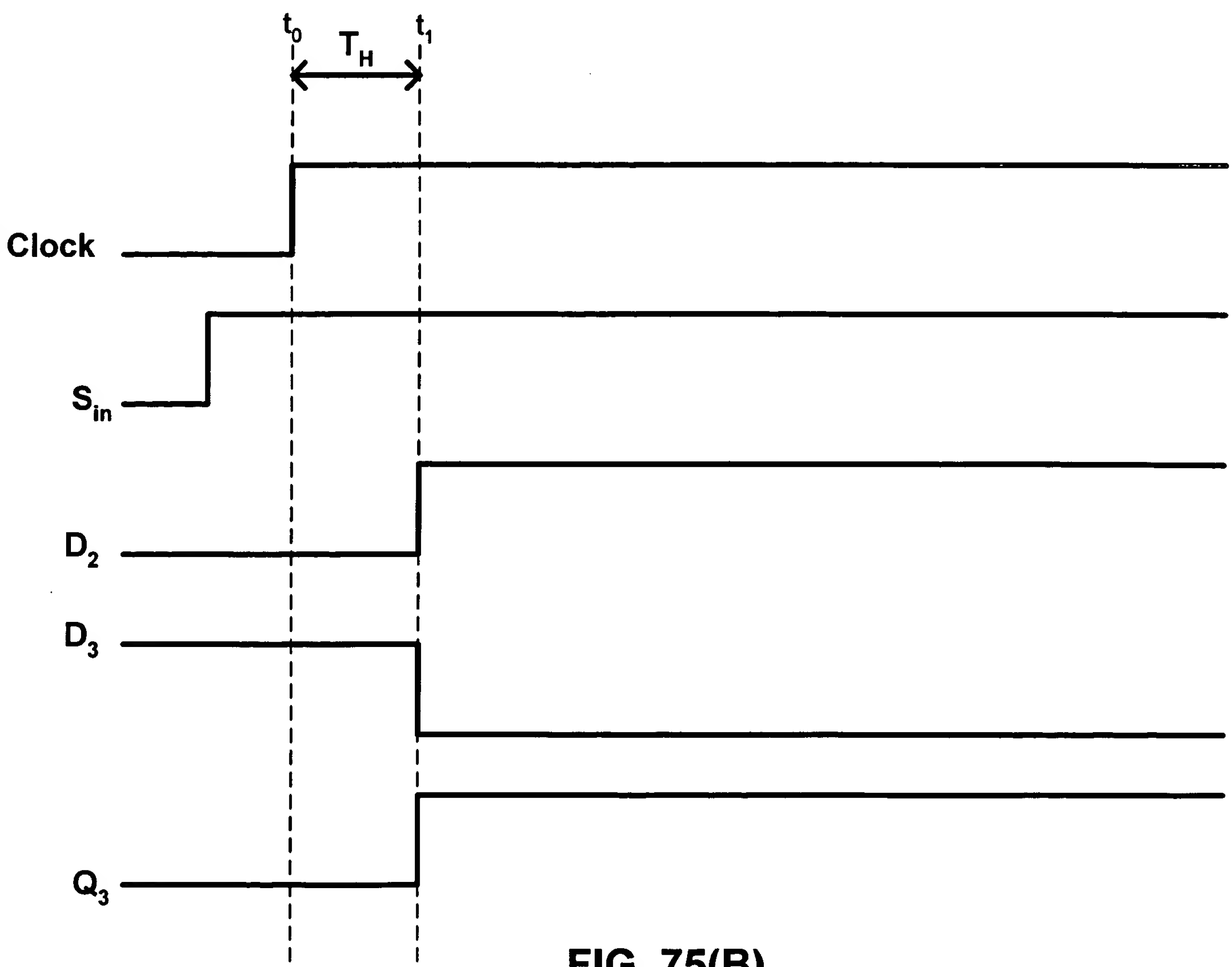


FIG. 75(B)

MULTIPLE FPGA MAPPING FOR SHIFT REGISTER

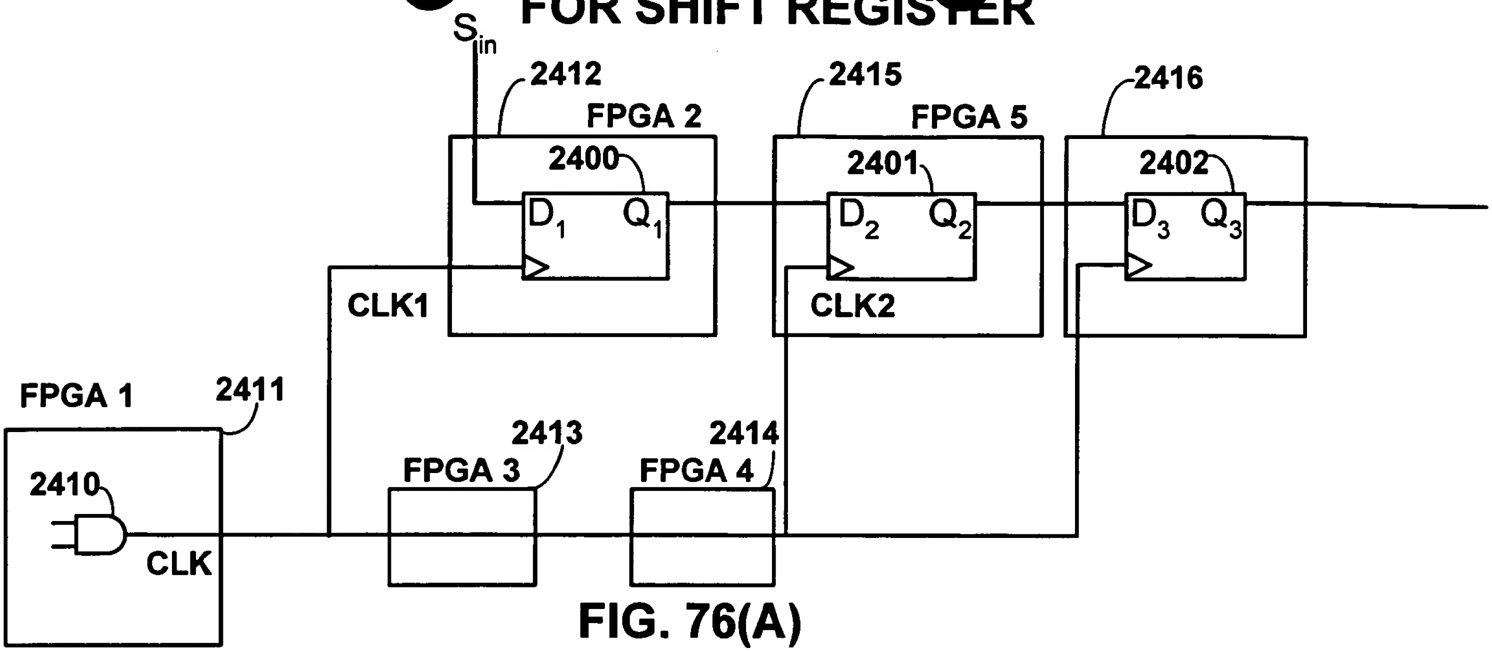
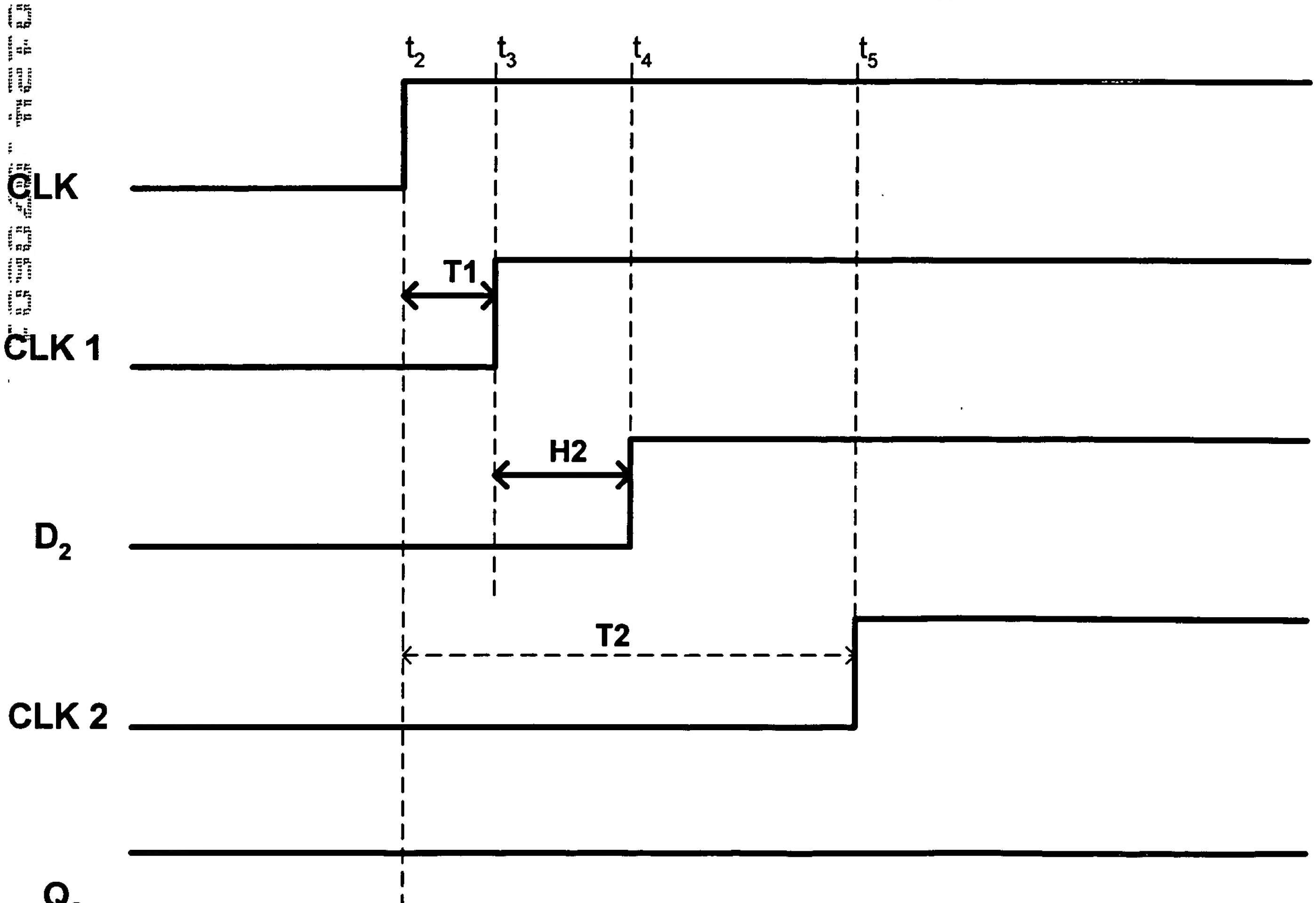


FIG. 76(A)

HOLD TIME VIOLATION BY LONG CLOCK SKEW



T2 > T1 + H2

FIG. 76(B)

CLOCK GLITCH PROBLEM

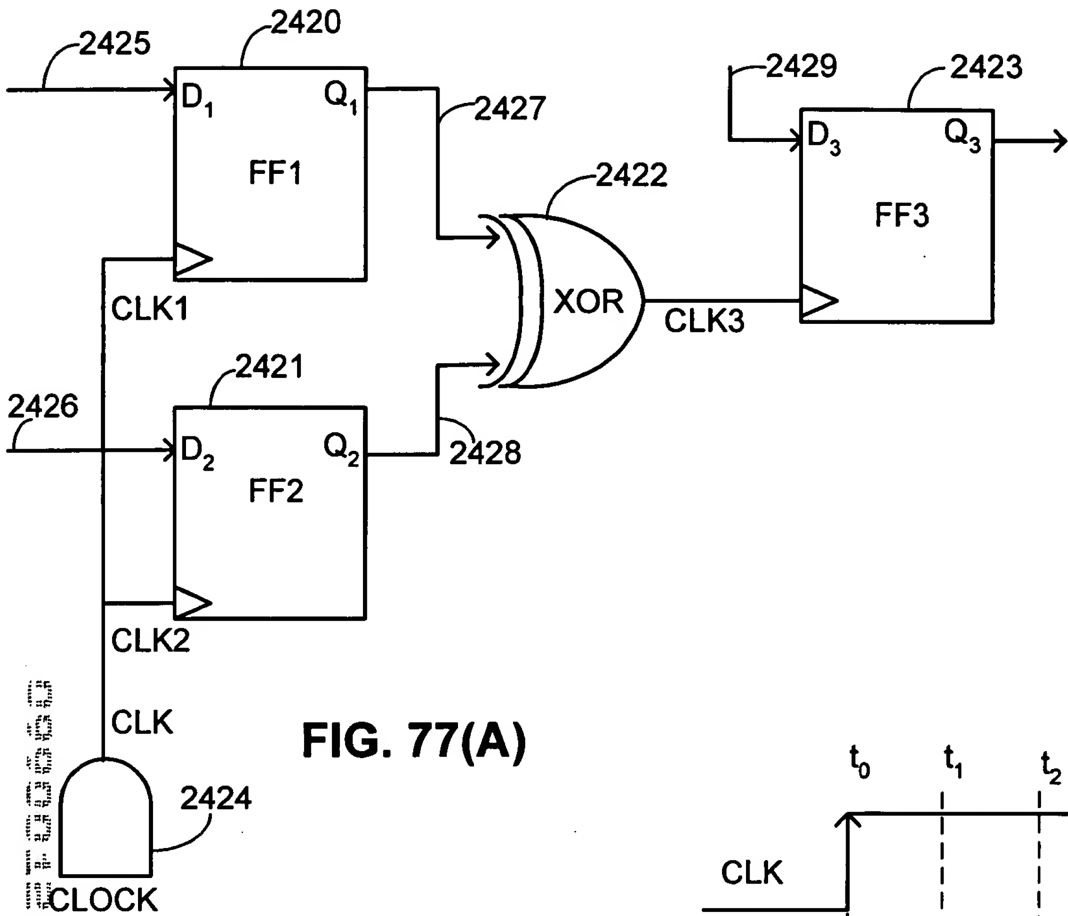


FIG. 77(A)

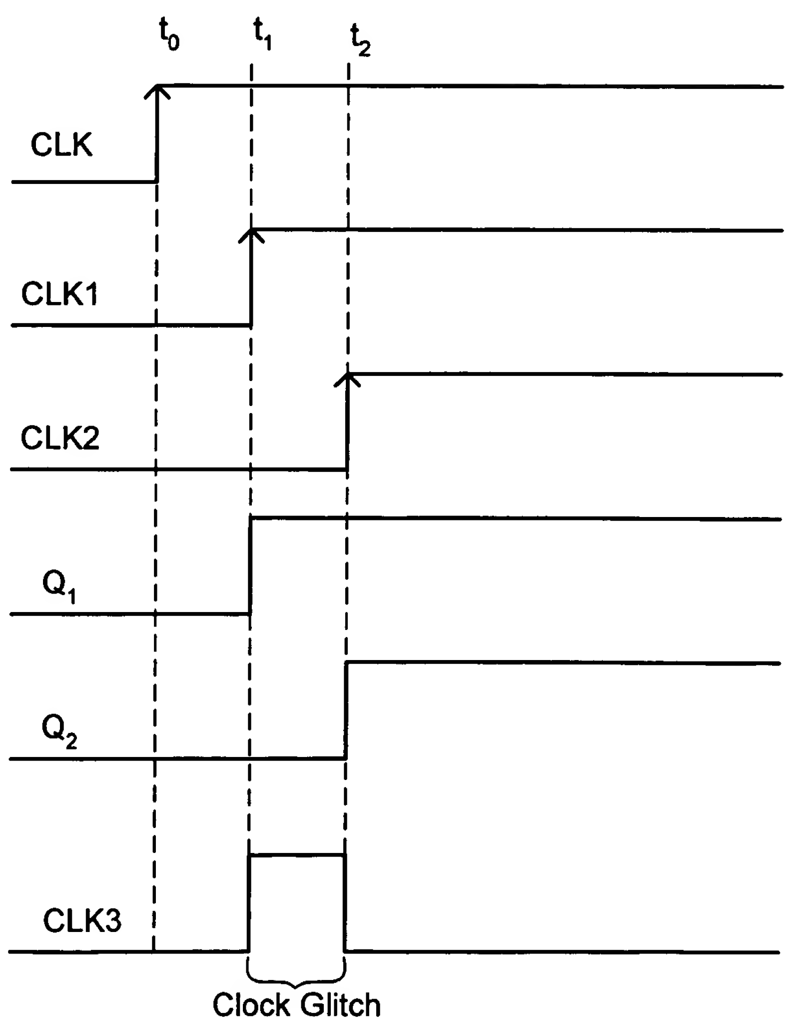
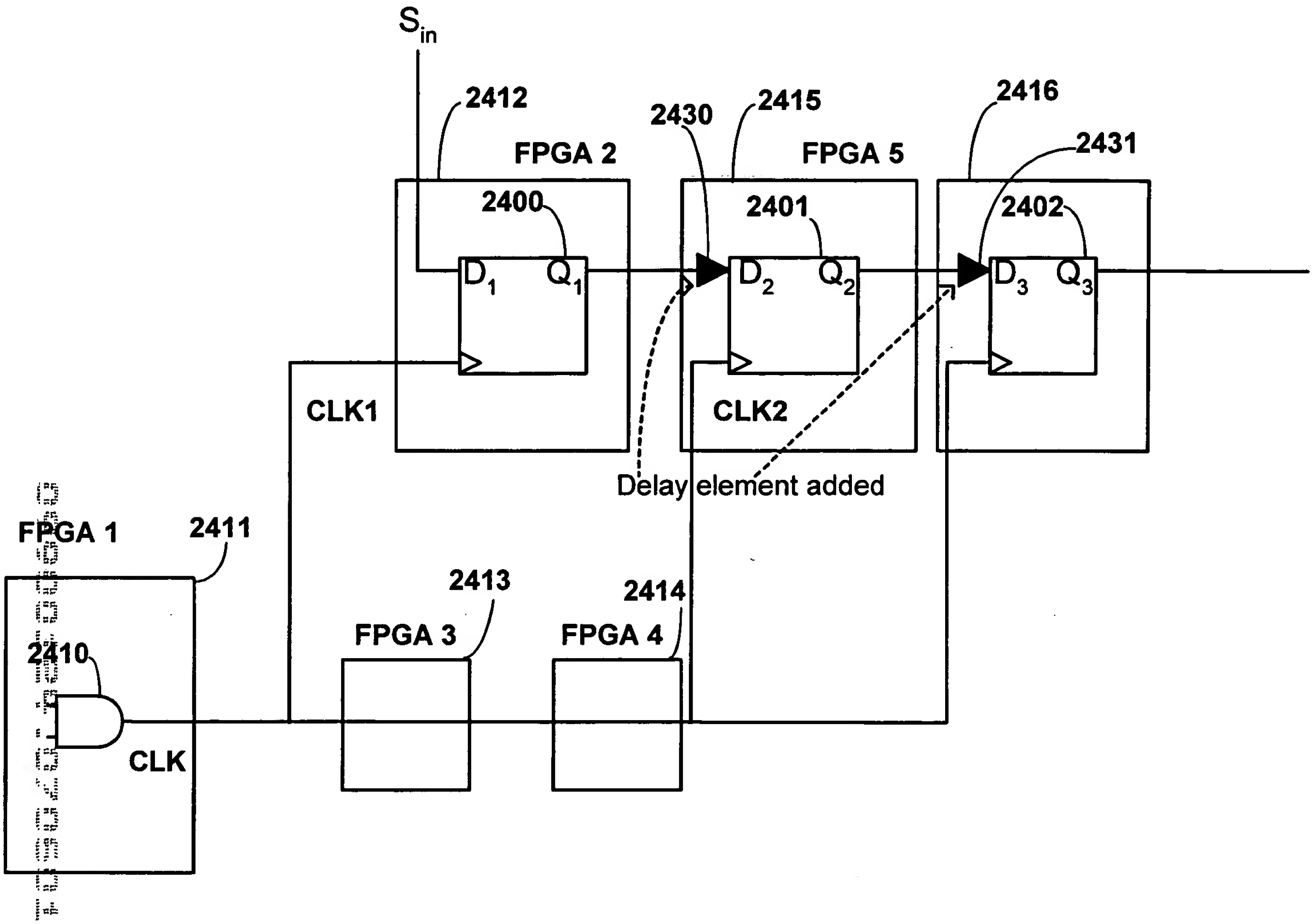


FIG. 77(B)

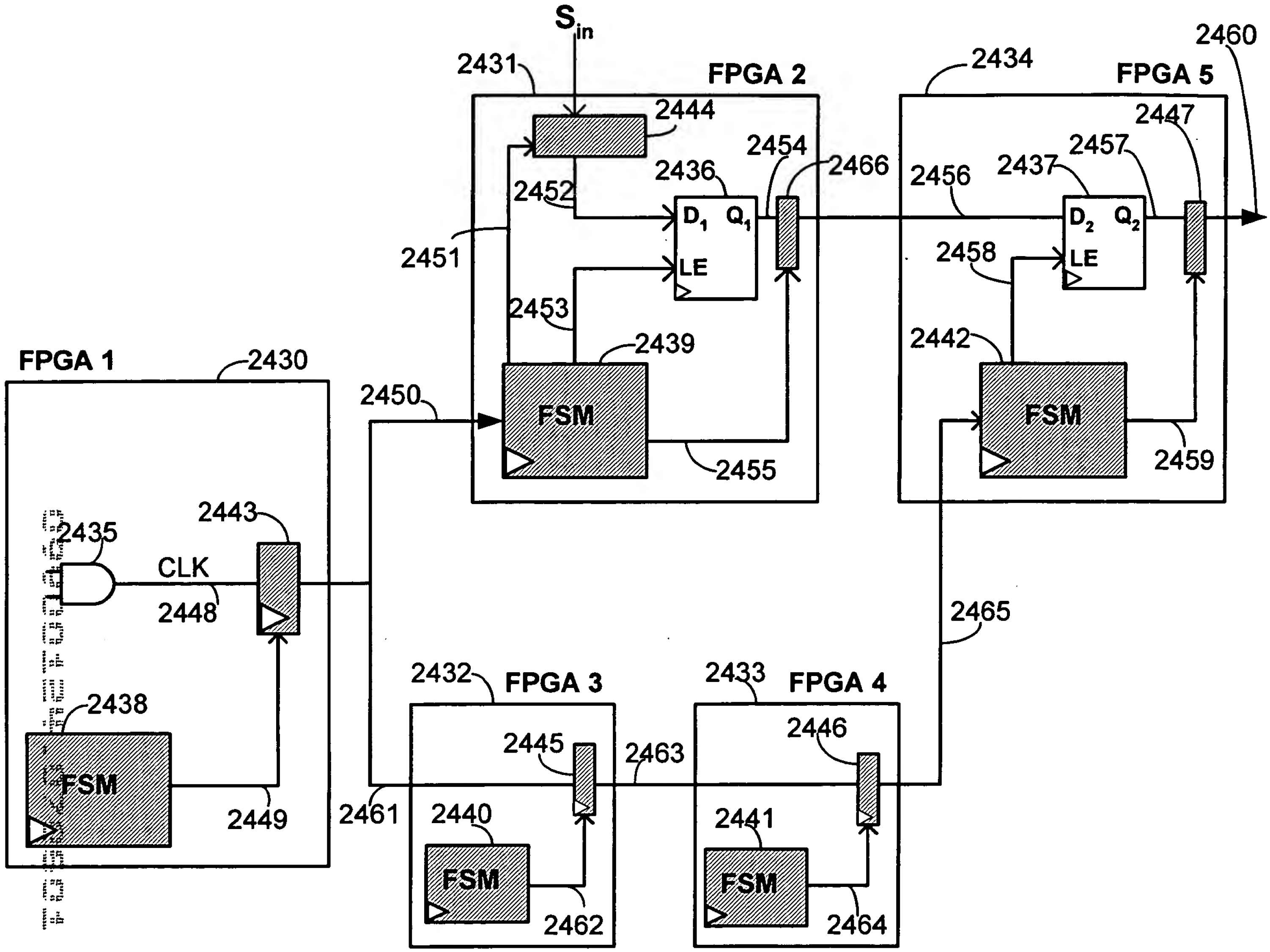
TIMING ADJUSTMENT BY ADDING DELAY



(Prior Art)

FIG. 78

GLOBAL RETIMING



Legend

Controlled by the global reference clock.

FSM and I/O registers for retiming control.

(Prior Art)

FIG. 79

TIGF LATCH

Original Latch

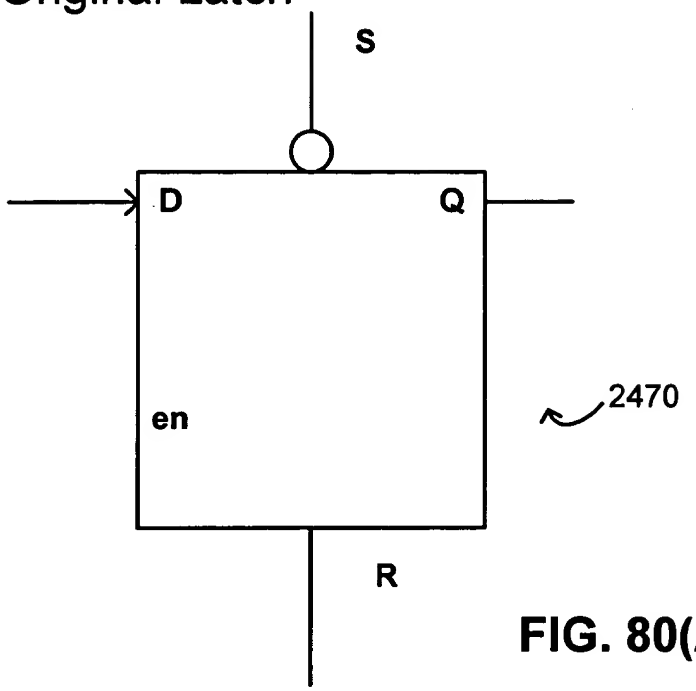


FIG. 80(A)

TIGF Latch

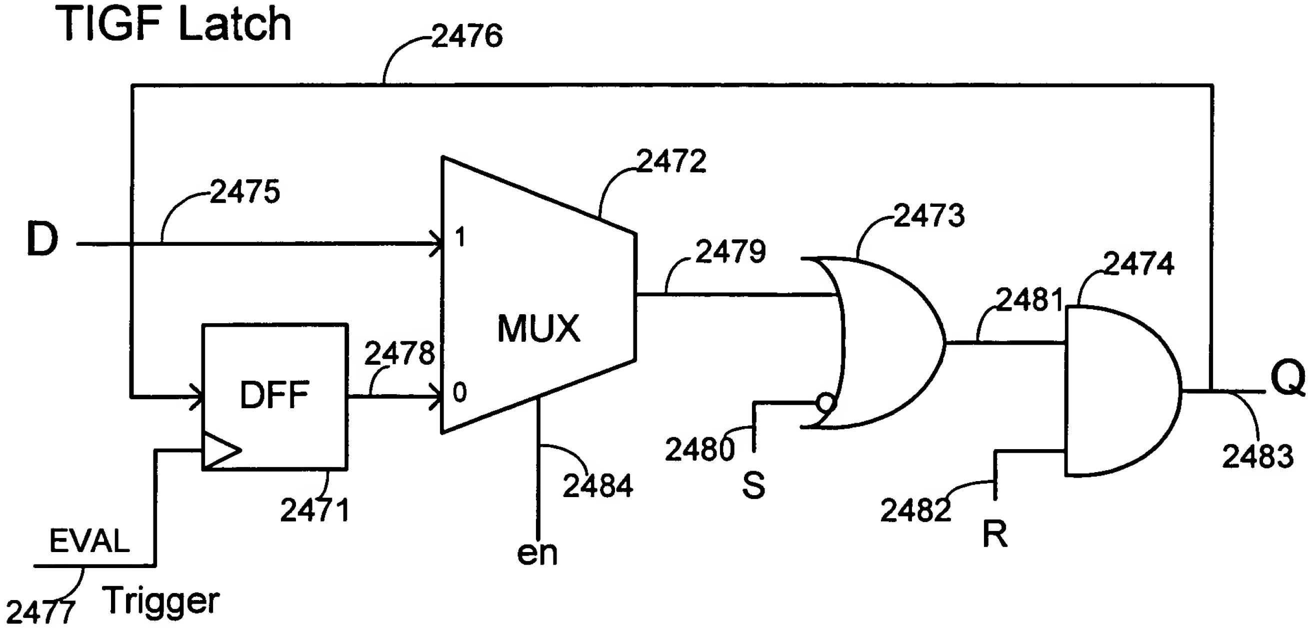


FIG. 80(B)

TIGF DFF

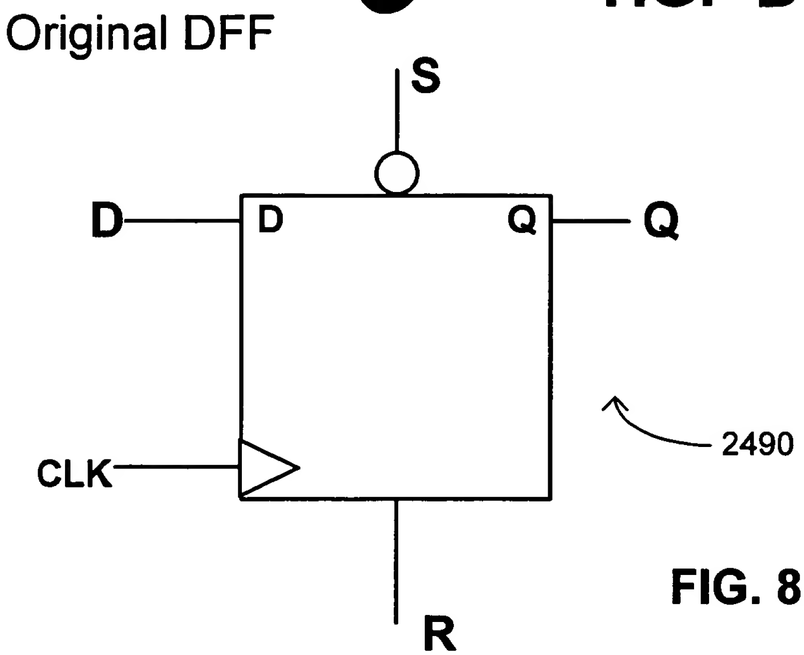


FIG. 81(A)

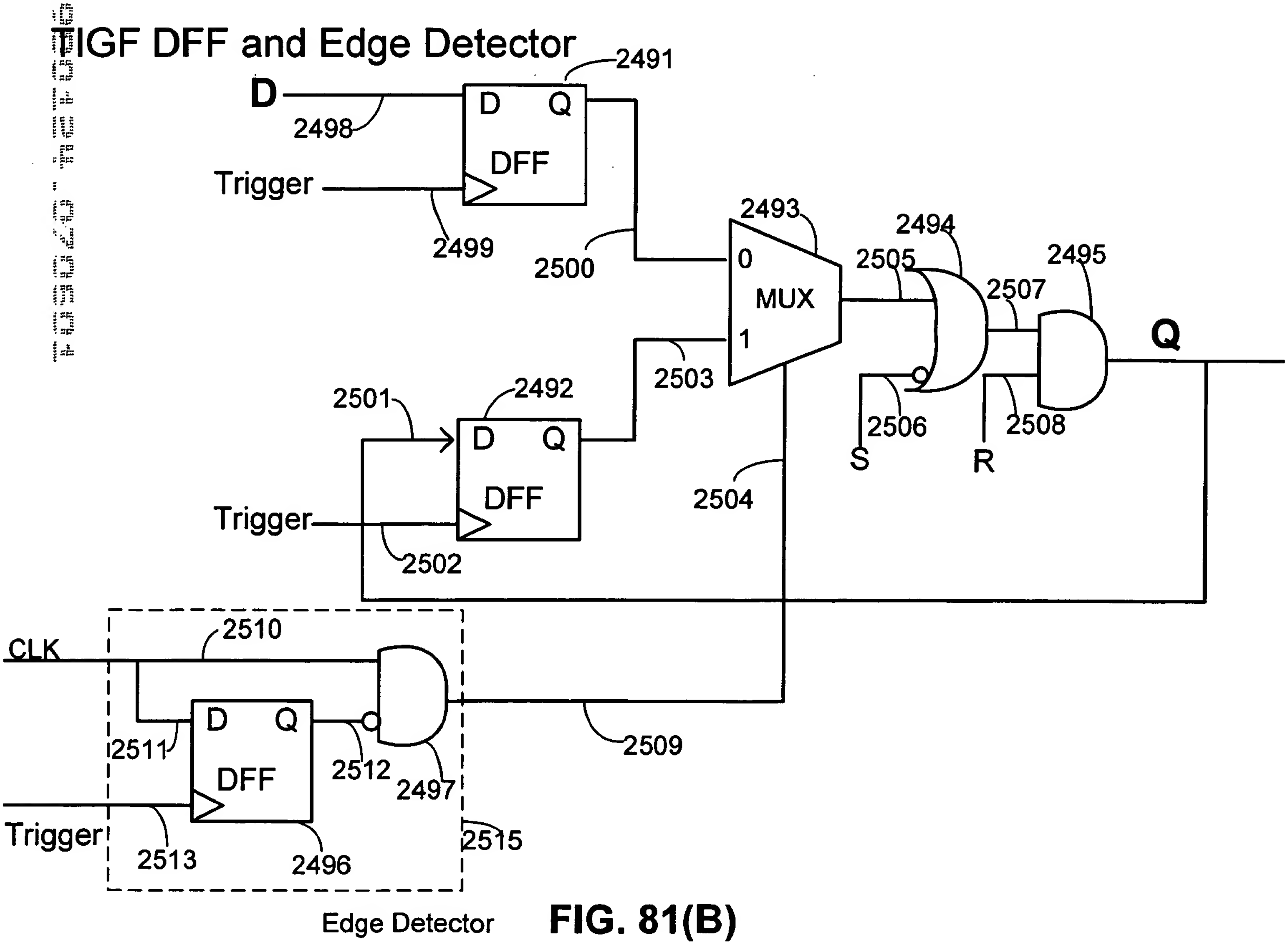


FIG. 81(B)

GLOBAL TRIGGER SIGNAL

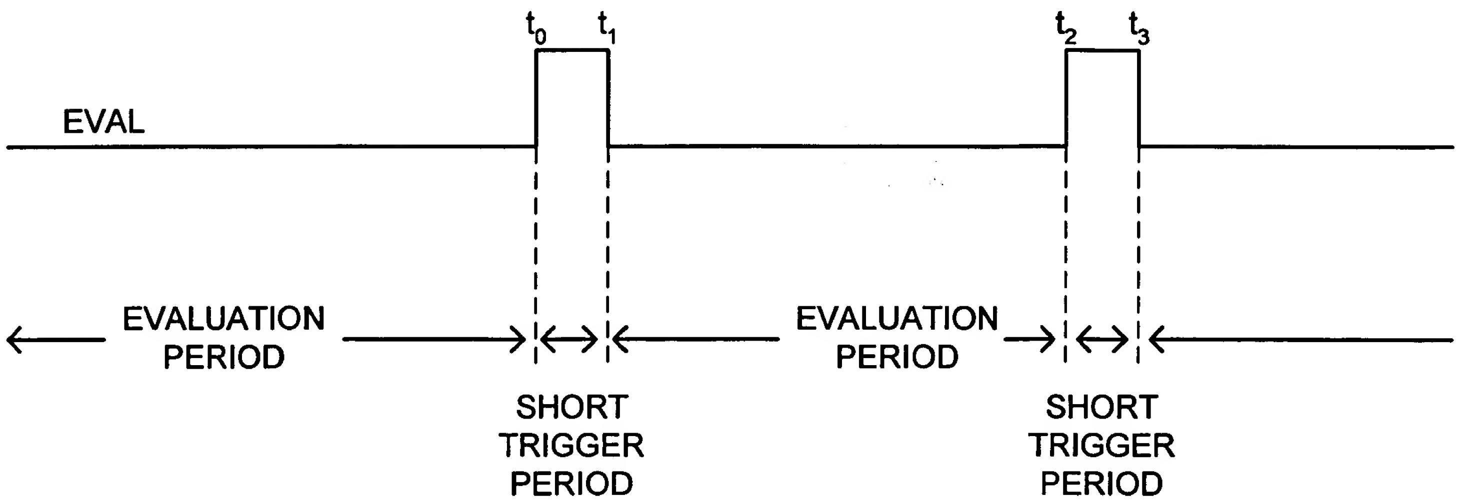


FIG. 82

RCC System

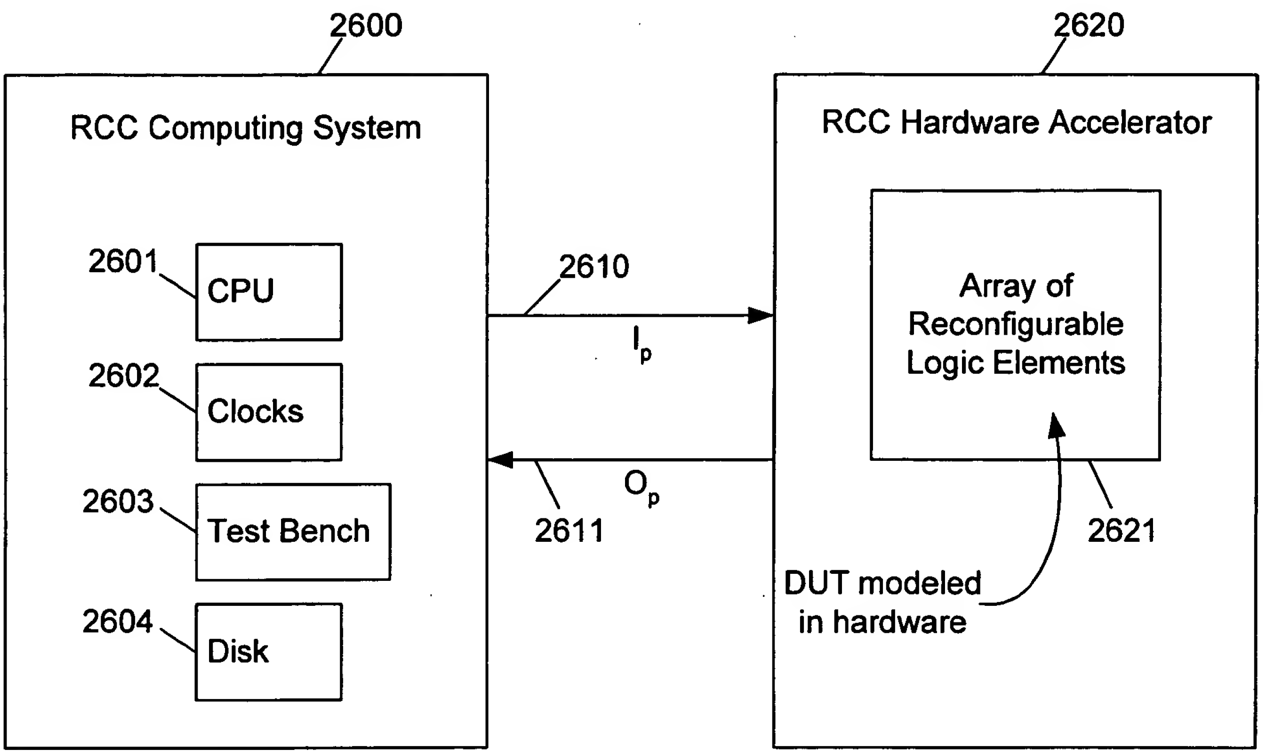


FIG. 83

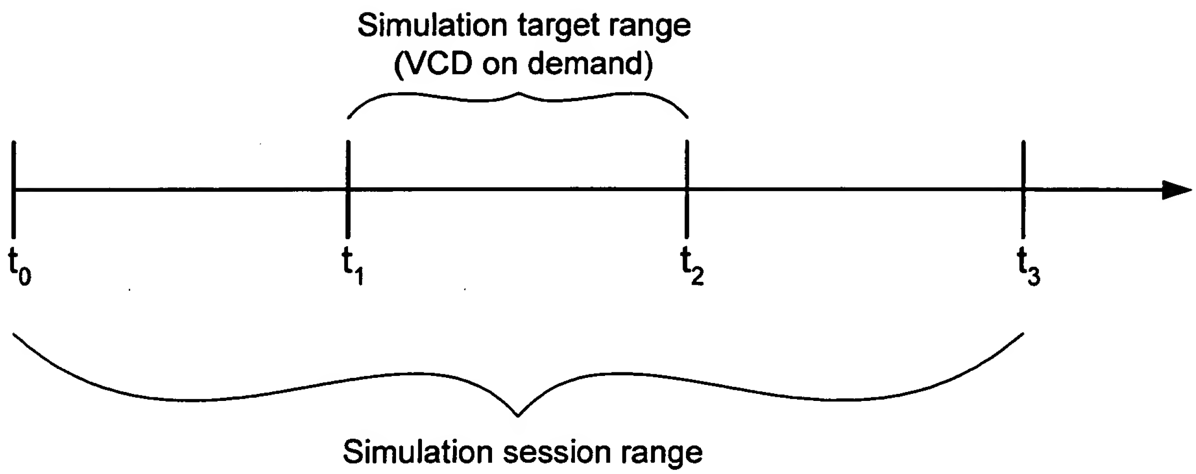

Simulation target range
(VCD on demand)
t_0
t_1
t_2
t_3
Simulation session range

FIG. 84

SINGLE-ROW FPGA PER BOARD

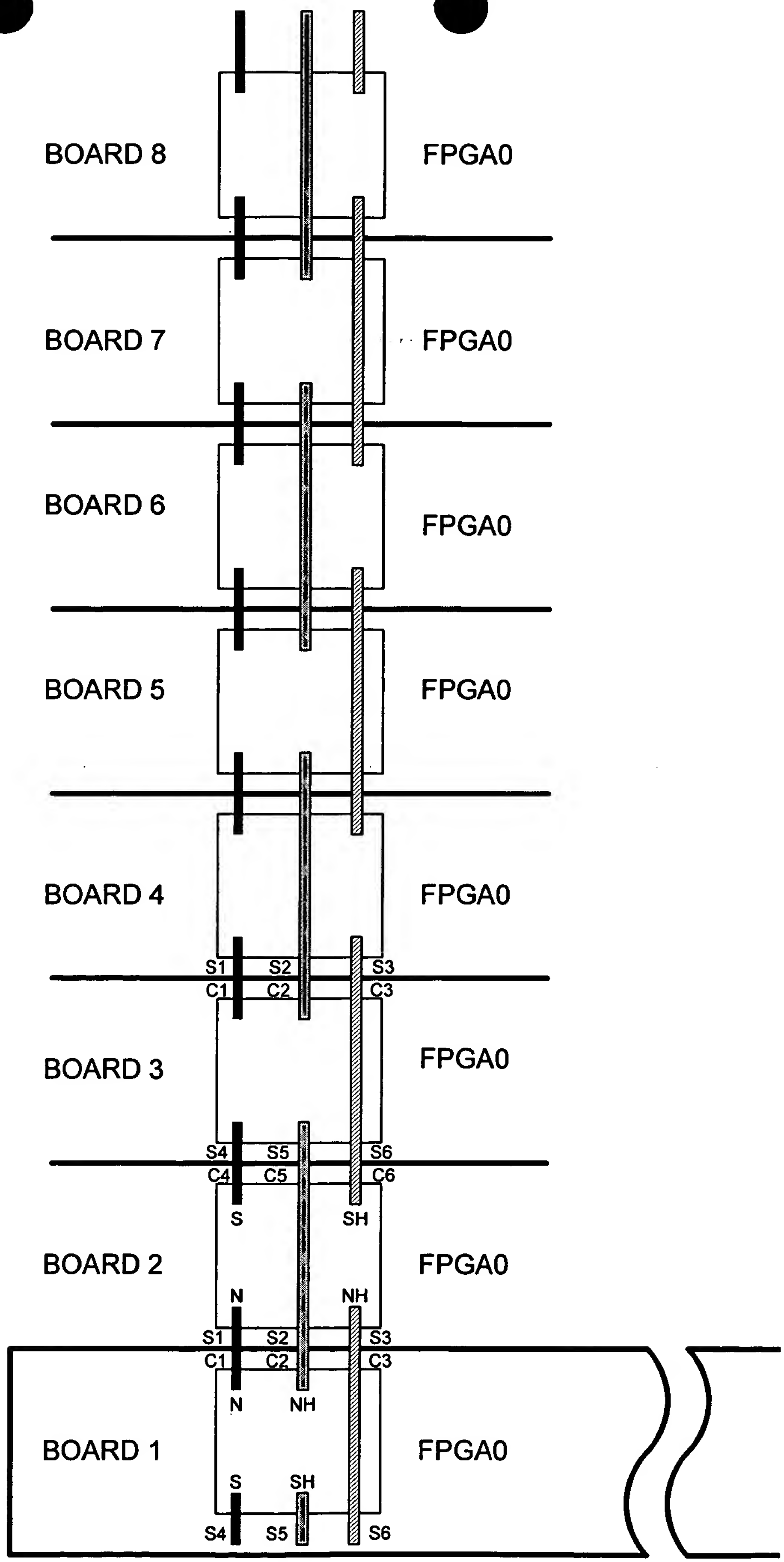


FIG. 85

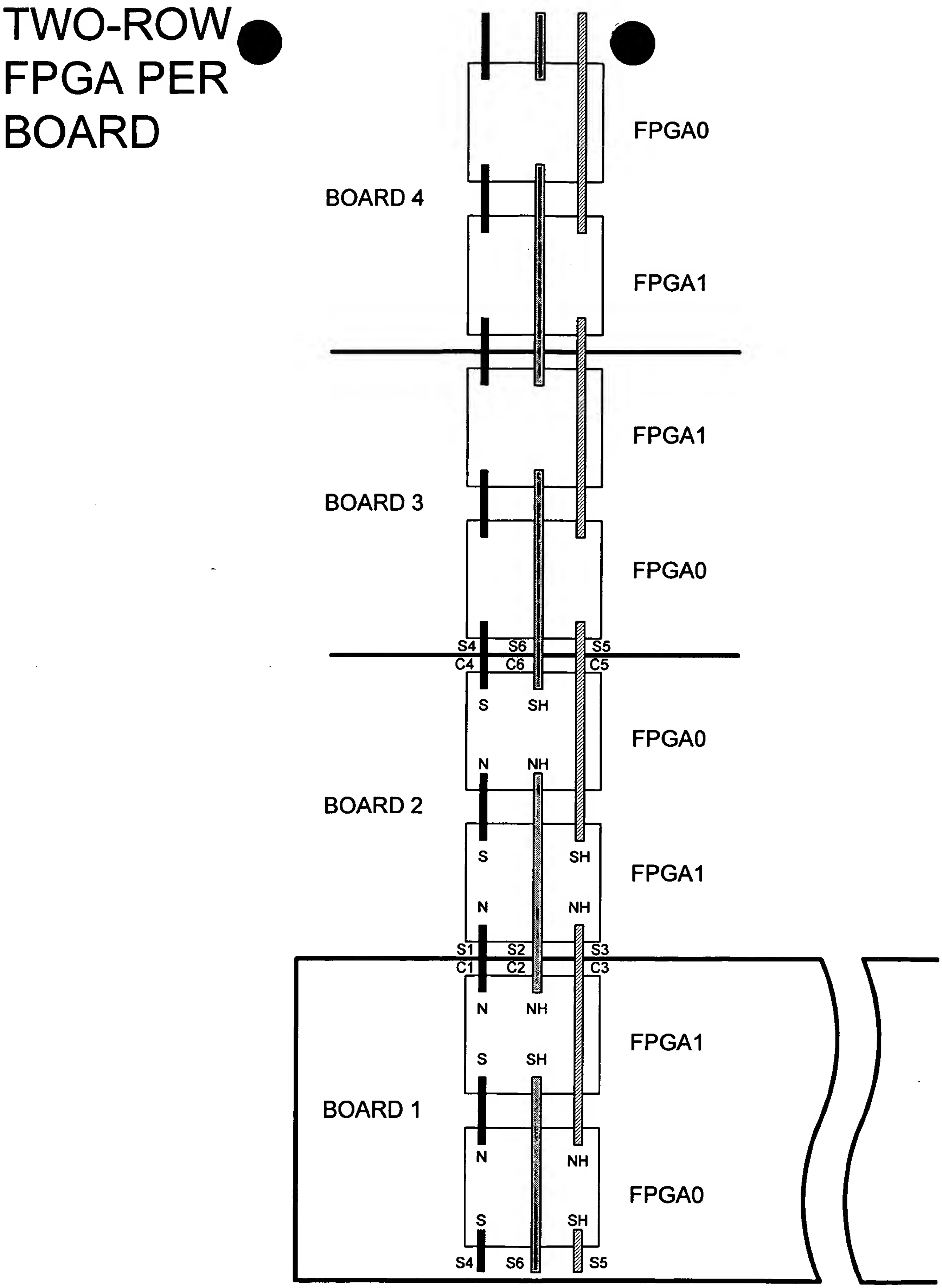

TWO-ROW FPGA PER BOARD
FPGA0
BOARD 4
FPGA1
FPGA1
BOARD 3
FPGA0
S4
S6
S5
C4
C6
C5
S
SH
FPGA0
N
NH
BOARD 2
S
SH
FPGA1
N
NH
S1
S2
S3
C1
C2
C3
N
NH
FPGA1
S
SH
BOARD 1
N
NH
FPGA0
S
SH
S4
S6
S5

FIG. 86

THREE-ROW FPGA PER BOARD

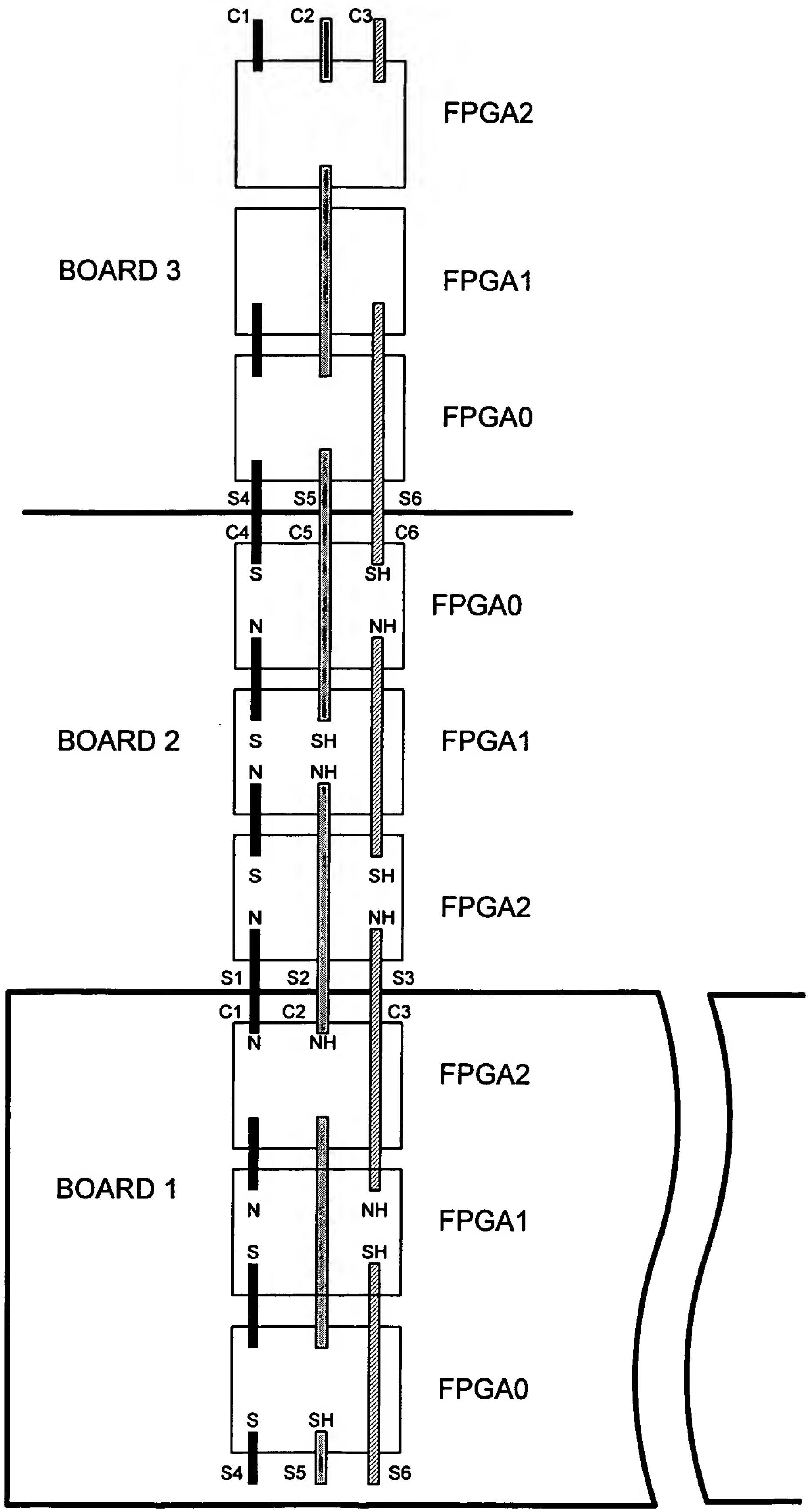


FIG. 87

FOUR-ROW FPGA PER BOARD

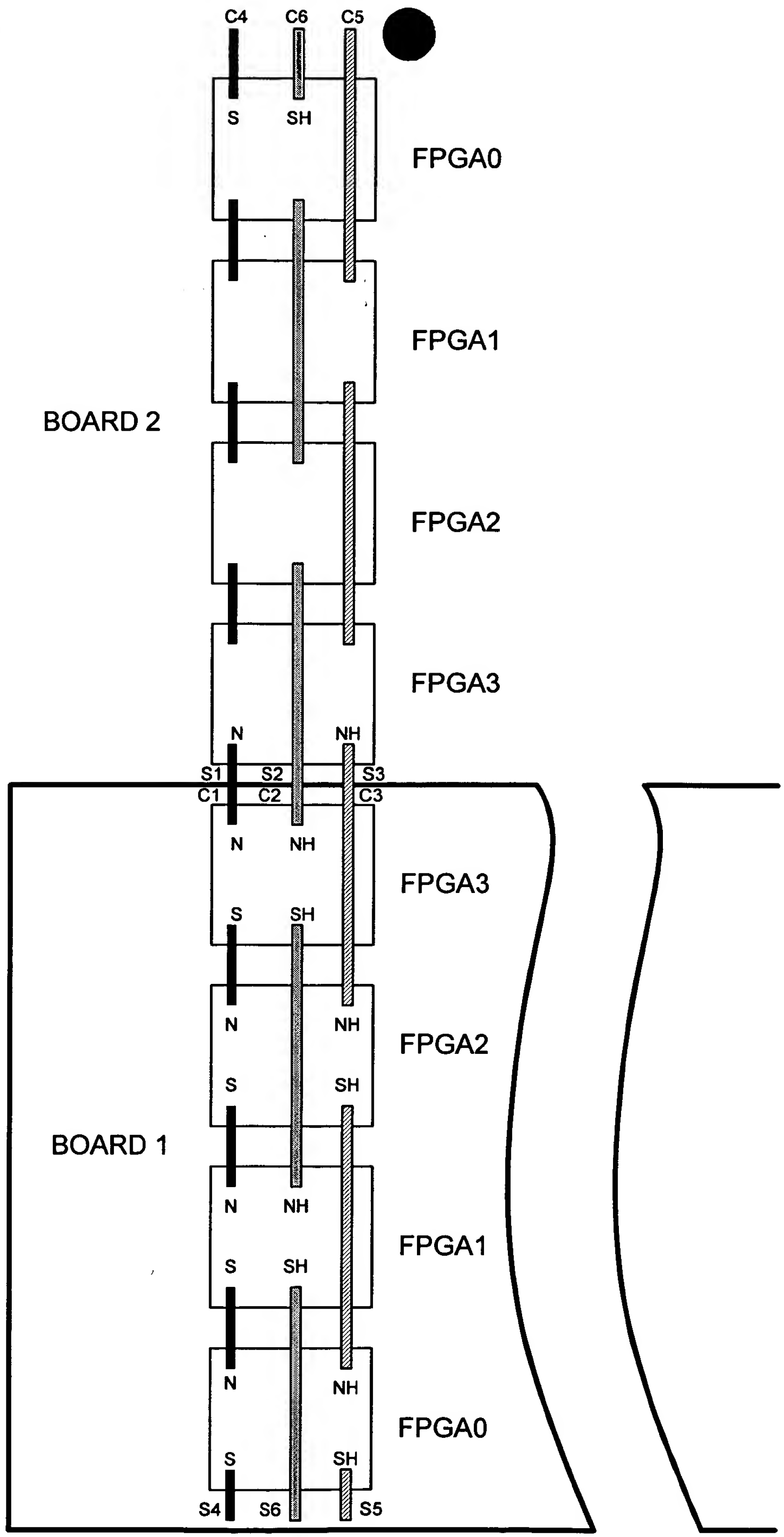


FIG. 88

INTERCONNECT FOR THREE-ROW PER BOARD

I/O Signals	Odd Board	Even Board	Common Board
	Connector-Group Pin-position	Connector-Group Pin-position	Connector-Group Pin-position
FPGA2_N	C1	S1	C1, S1
FPGA2_NH	C2	S3	C2, S3
FPGA1_NH	C3	S2	C3, S2
FPGA0_S	S4	C4	C4, S4
FPGA0_SH	S5	C6	C6, S5
FPGA1_SH	S6	C5	C5, S6

FIG. 89

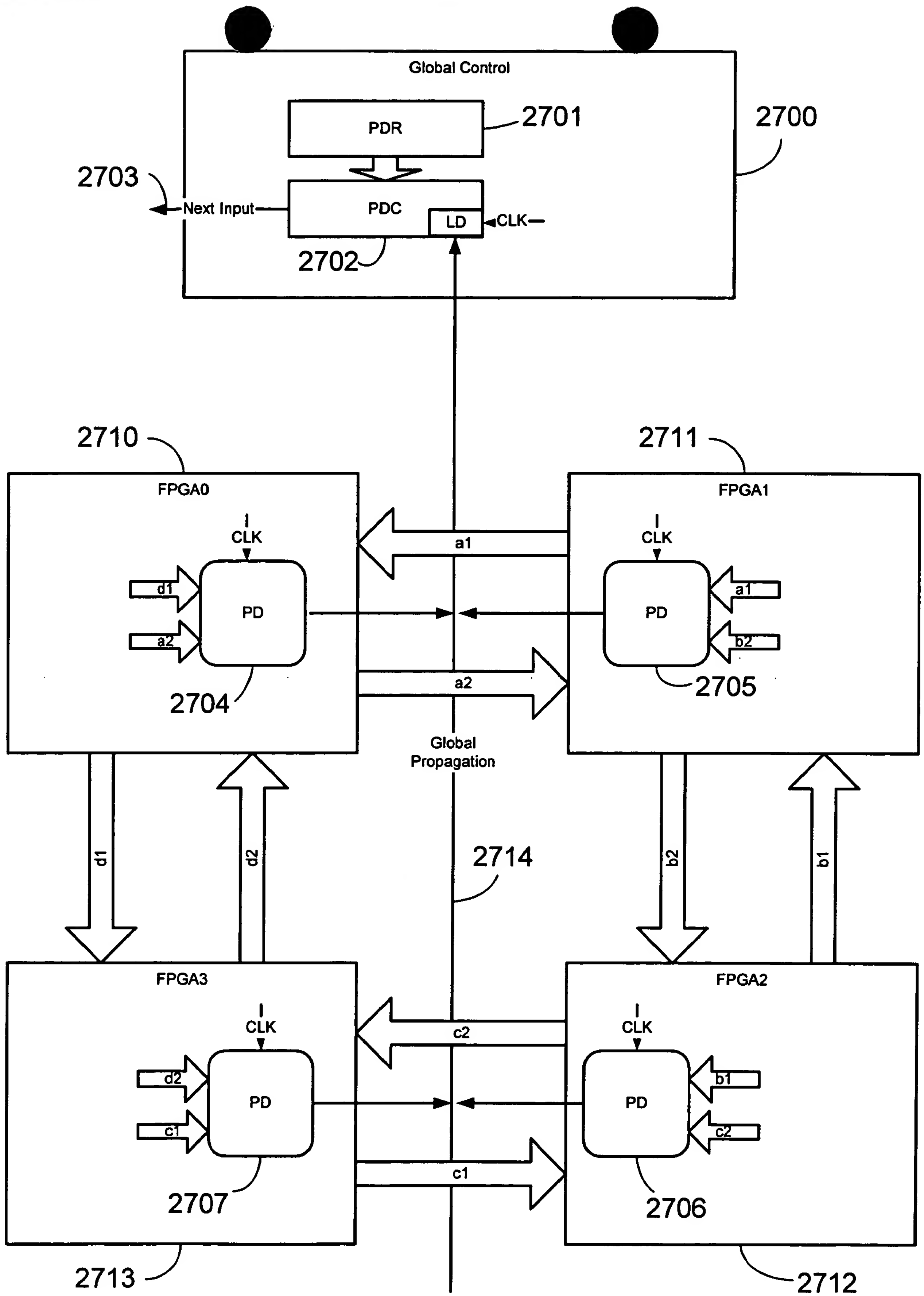

Global Control
PDR
2701
2700
2703
Next Input
PDC
LD
CLK
2702
2710
2711
FPGA0
FPGA1
CLK
CLK
a1
d1
PD
PD
a1
a2
b2
a2
2704
2705
Global
Propagation
d1
d2
2714
b2
b1
FPGA3
FPGA2
CLK
CLK
c2
d2
PD
PD
b1
c1
c2
c1
2707
2706
2713
2712

FIG. 90

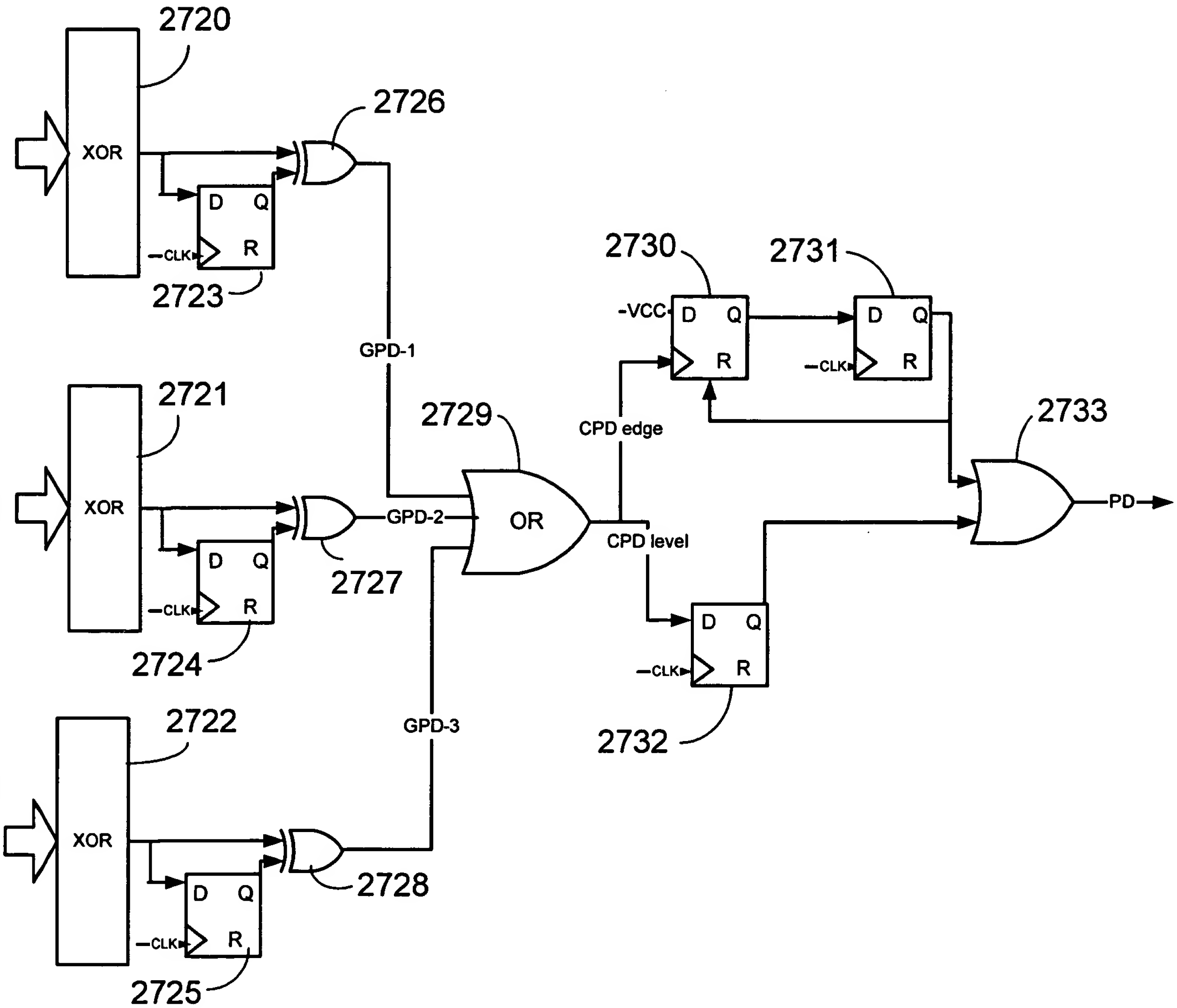

2720
XOR
D
Q
CLK
R
2723
2726
GPD-1
2721
XOR
D
Q
CLK
R
2724
GPD-2
2727
2722
XOR
D
Q
CLK
R
2725
2728
GPD-3
2729
OR
CPD edge
CPD level
2730
-VCC
D
Q
R
2731
D
Q
CLK
R
D
Q
CLK
R
2732
2733
PD

FIG. 91

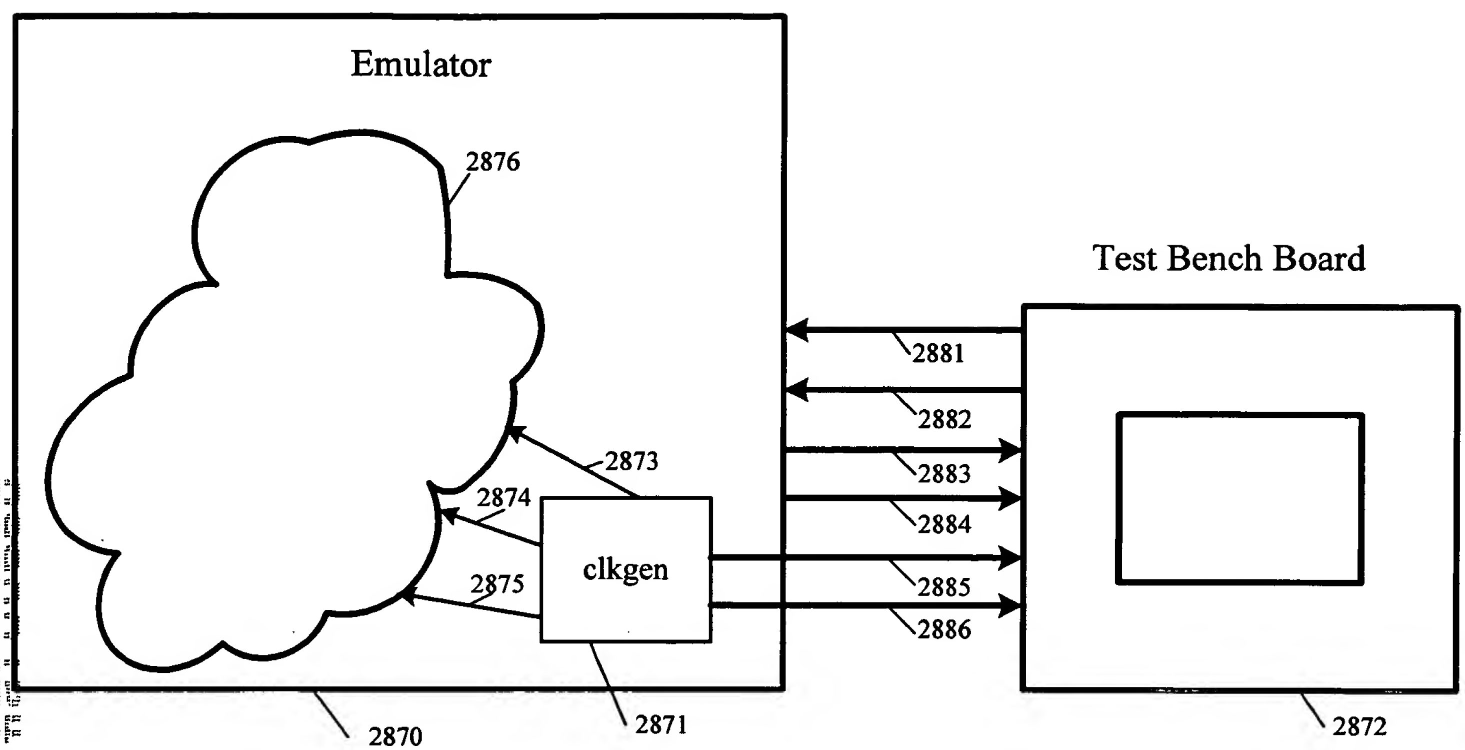

Emulator
2876
Test Bench Board
2881
2882
2873
2883
2874
2884
clkgen
2885
2875
2886
2870
2871
2872

FIG. 92

Clock Specification

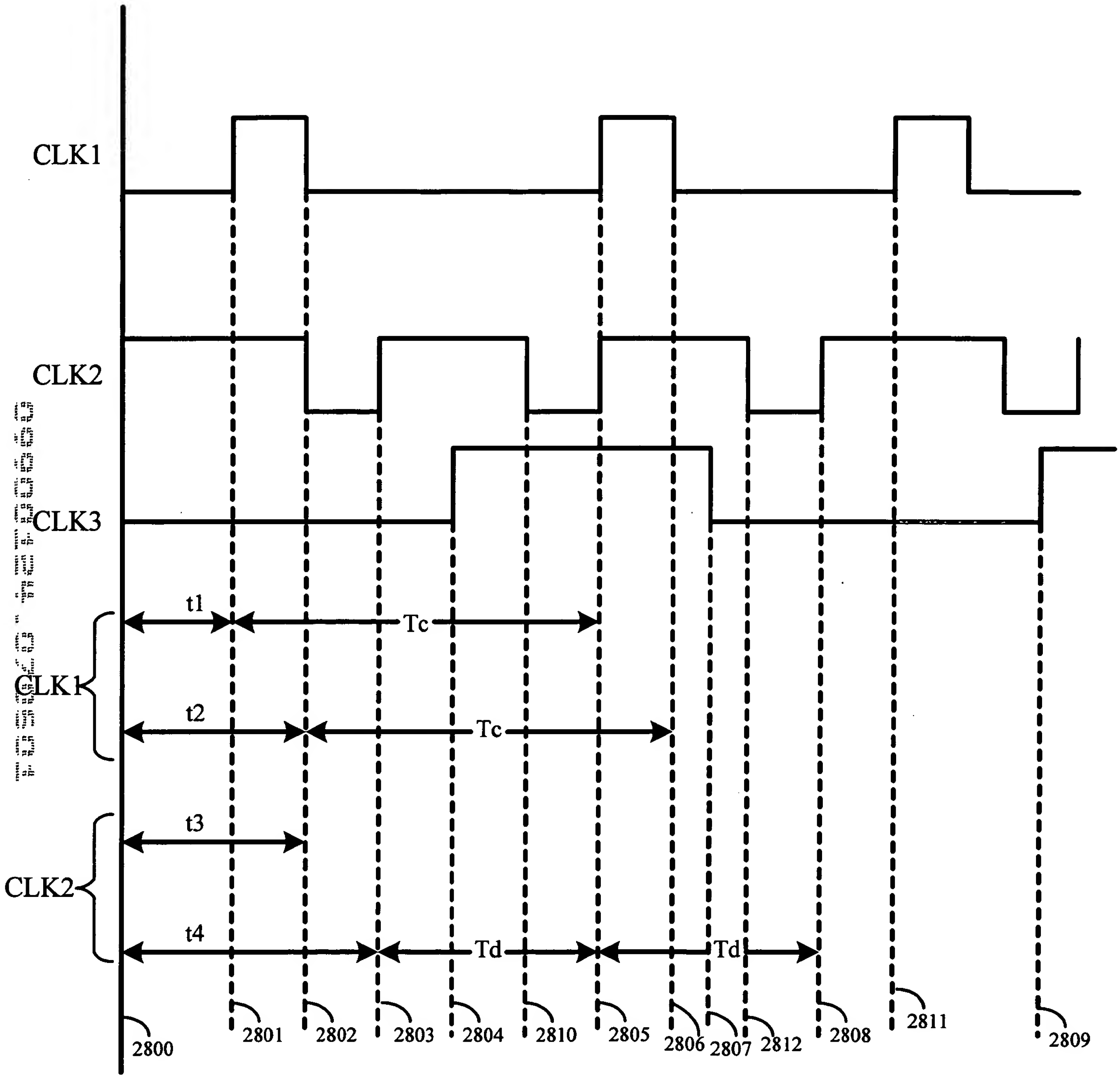


FIG. 93

Clock Generation Scheduler w/ Slices

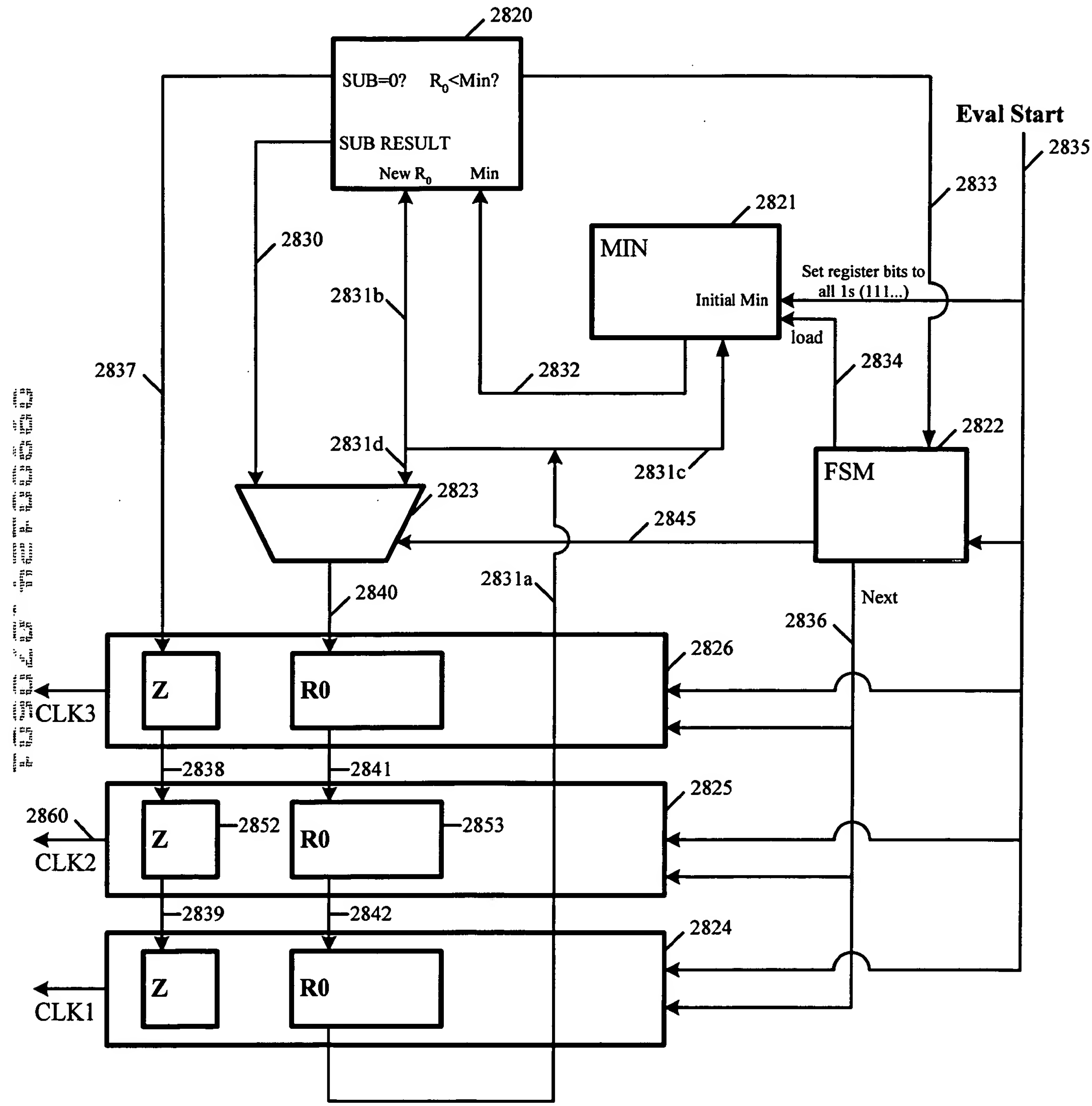


FIG. 94

Clock Generation Slice

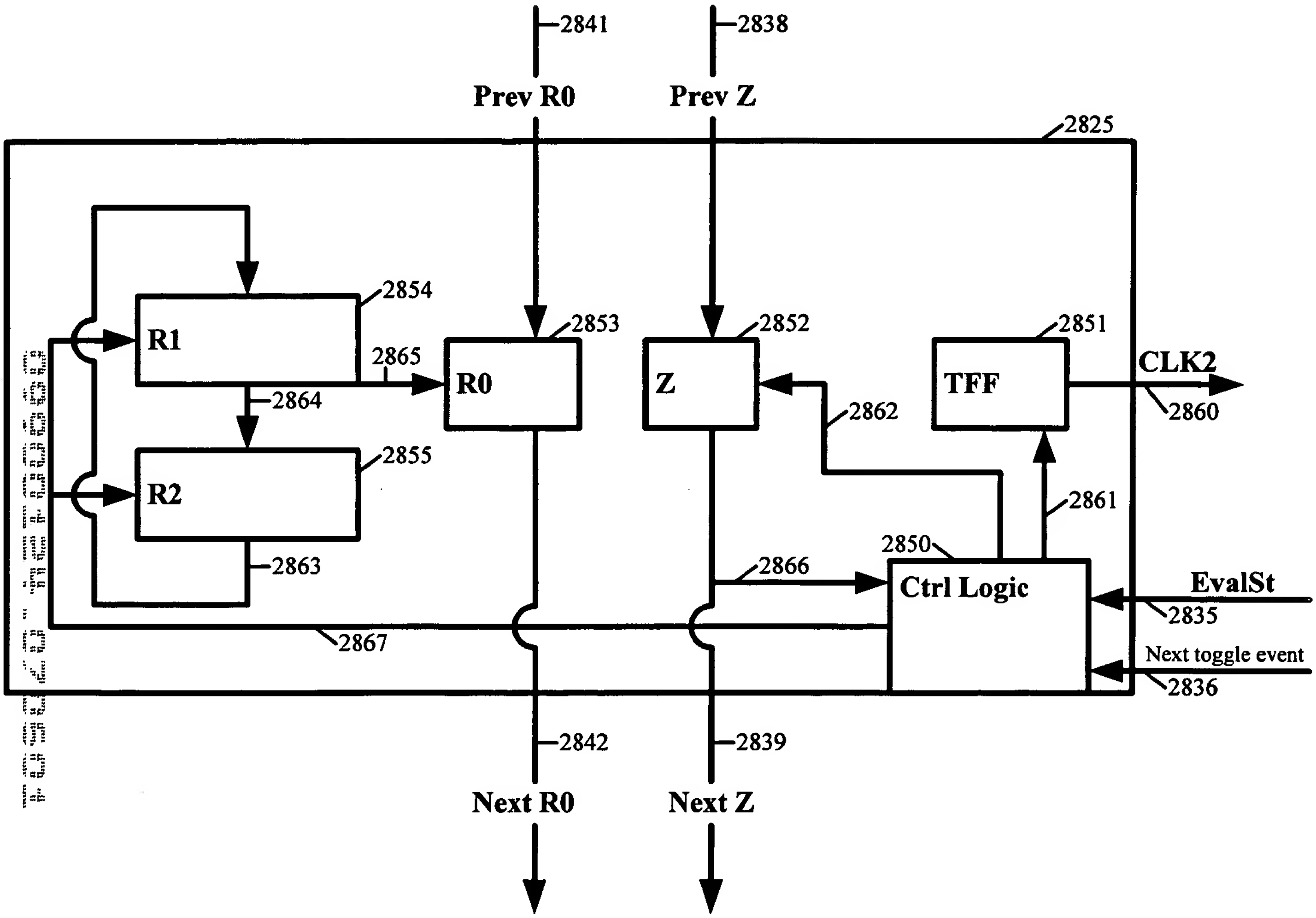


FIG. 95

Clock Generation Scheduler and Slices

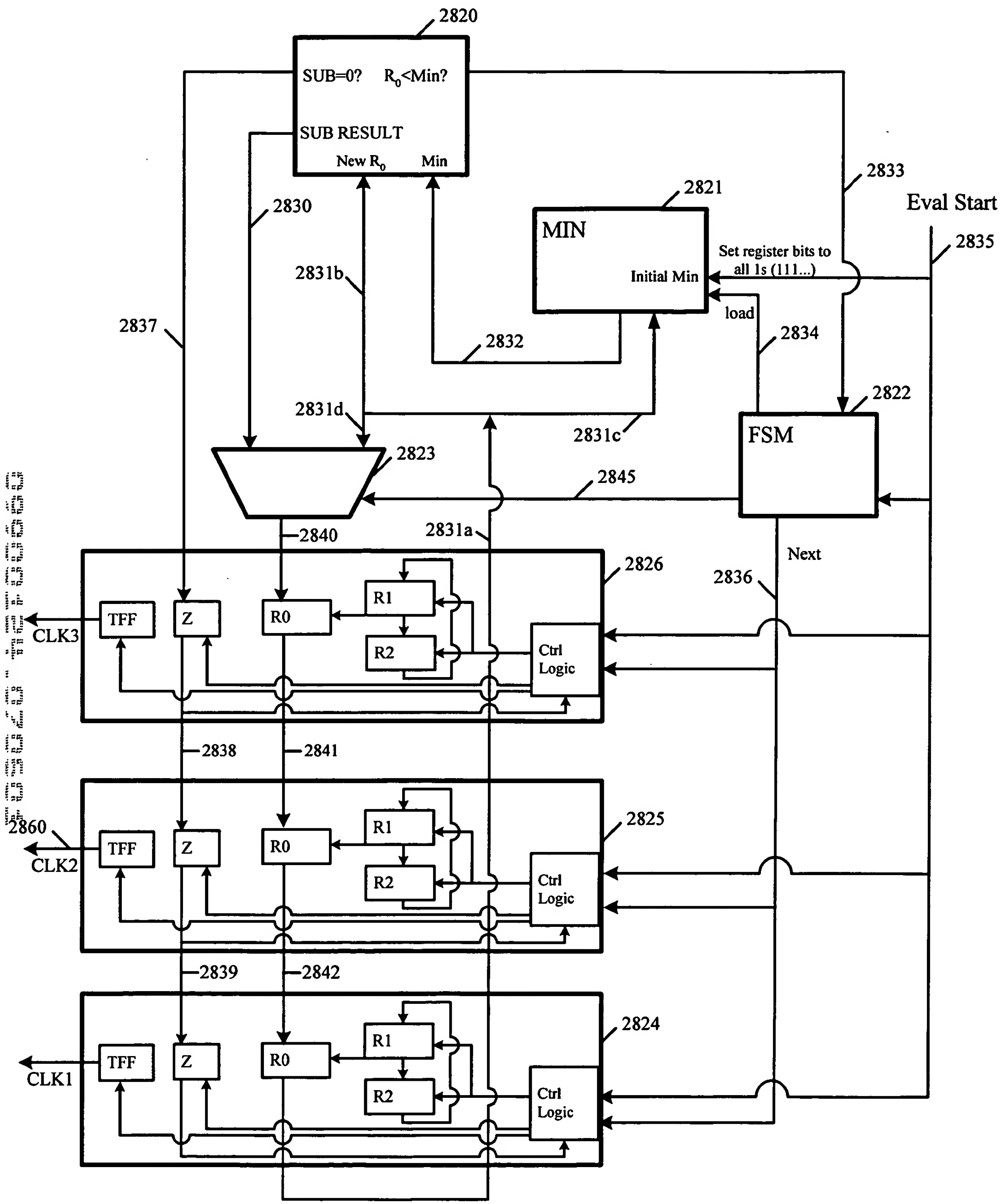


FIG. 96

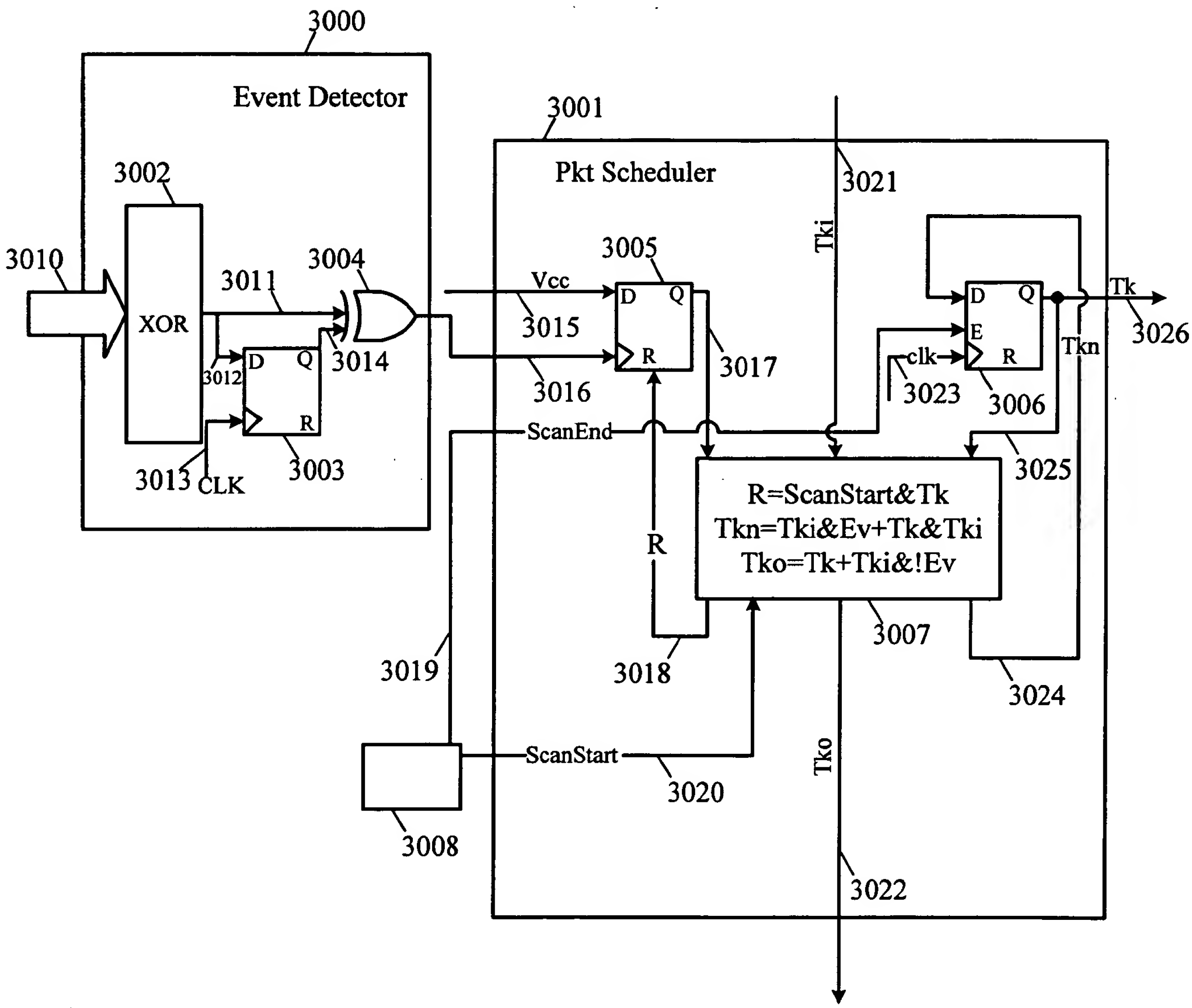
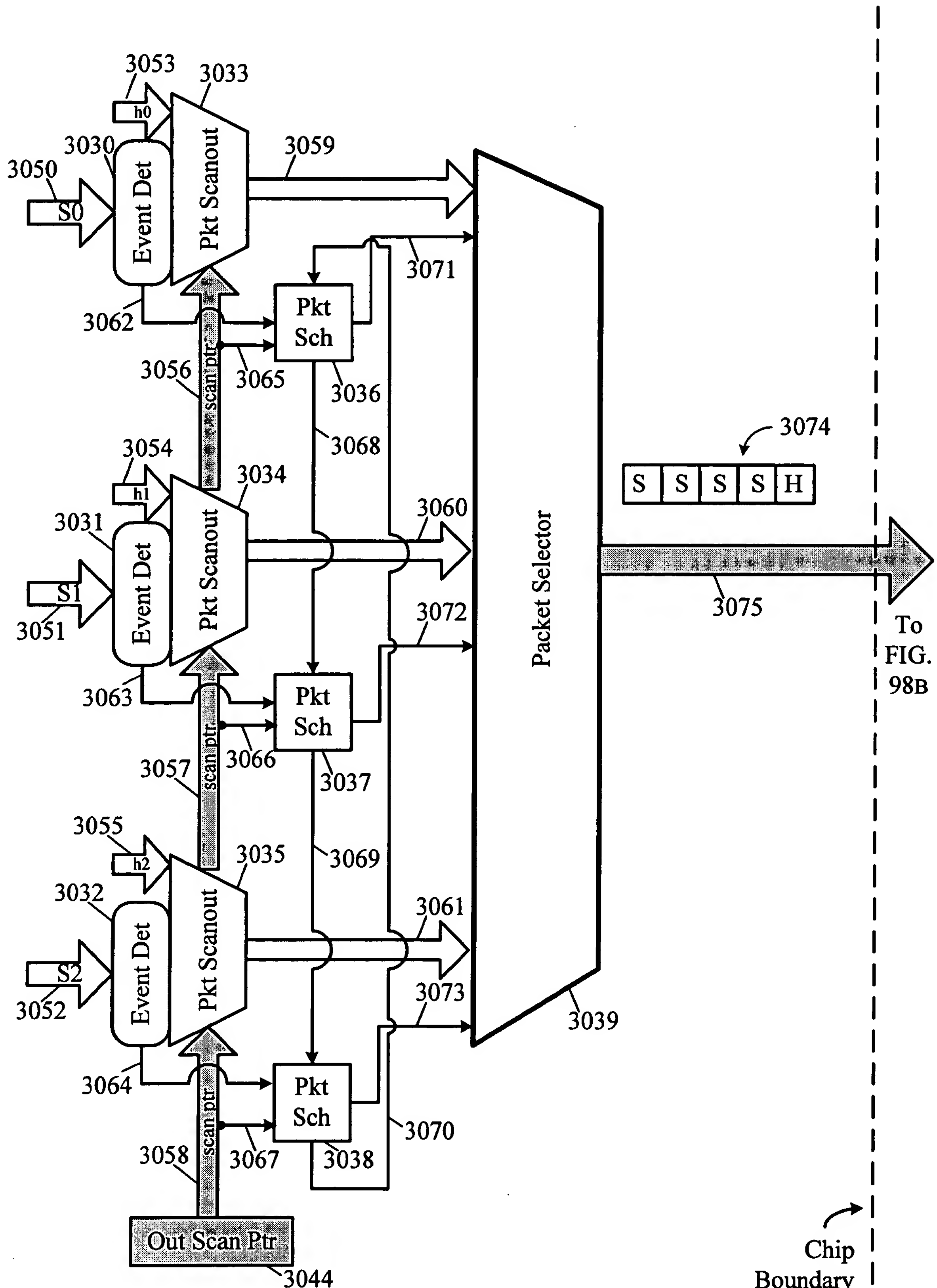

3000
Event Detector
3002
XOR
3010
3011
3004
3012
3014
3013
CLK
3003
3001
Pkt Scheduler
3021
Tki
3005
Vcc
3015
3016
3017
ScanEnd
3023
clk
3006
Tk
3026
Tkn
3025
R=ScanStart&Tk
Tkn=Tki&Ev+Tk&Tki
Tko=Tk+Tki&!Ev
R
3007
3018
3019
3024
ScanStart
3020
Tko
3008
3022

FIG. 97



S0
S1
S2
h0
h1
h2
Event Det
Pkt Scanout
Pkt Sch
scan ptr
Out Scan Ptr
Packet Selector
S S S S H
To FIG. 98B
Chip Boundary
3030
3031
3032
3033
3034
3035
3036
3037
3038
3039
3044
3050
3051
3052
3053
3054
3055
3056
3057
3058
3059
3060
3061
3062
3063
3064
3065
3066
3067
3068
3069
3070
3071
3072
3073
3074
3075

FIG. 98A

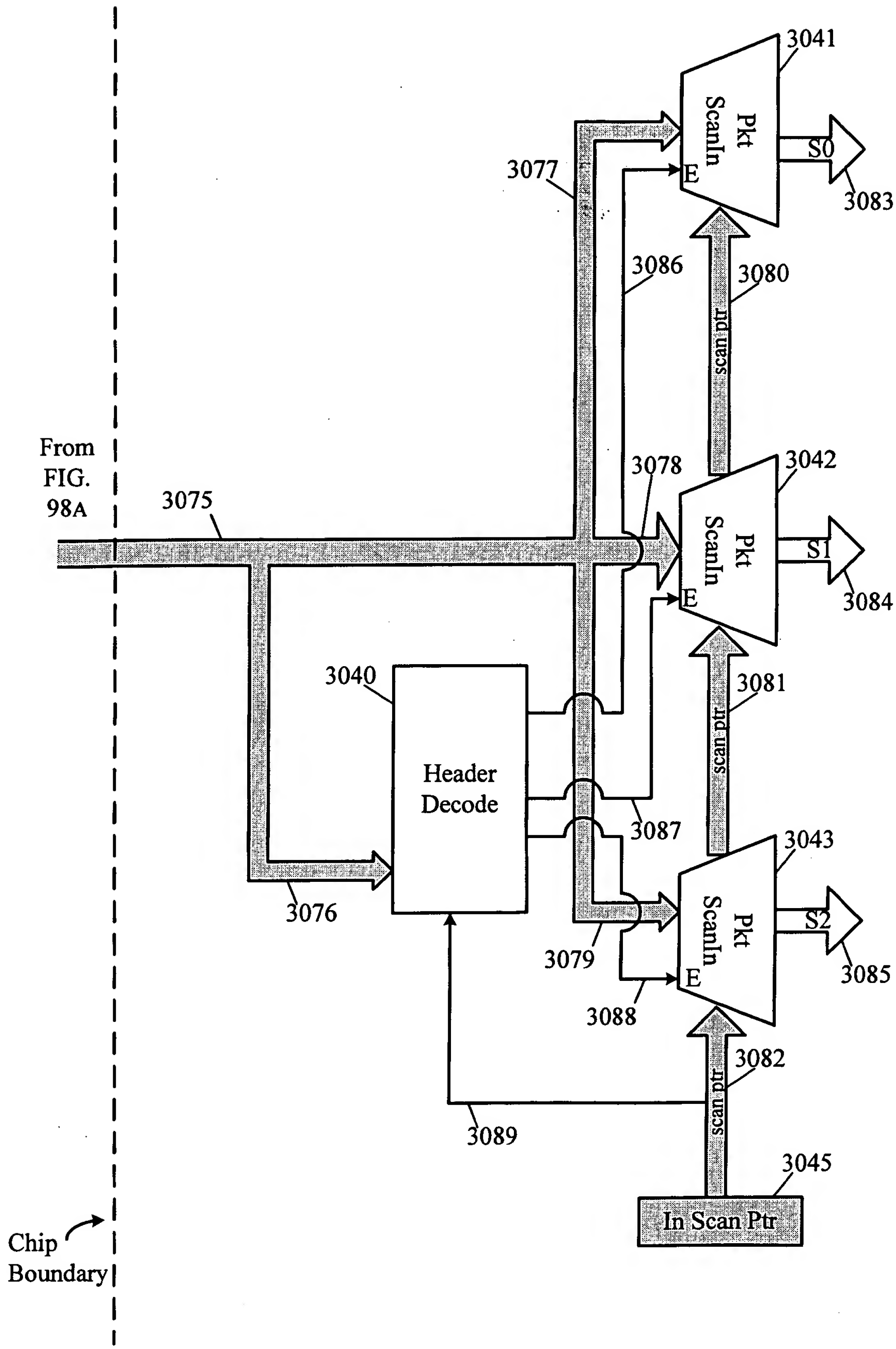

From FIG. 98A
Chip Boundary
3075
3076
3040
Header Decode
3077
3078
3079
3086
3087
3088
3089
3041
3042
3043
Pkt ScanIn
Pkt ScanIn
Pkt ScanIn
E
E
E
3080
3081
3082
scan ptr
scan ptr
scan ptr
S0
S1
S2
3083
3084
3085
3045
In Scan Ptr

FIG. 98B